Large Size InGaAs-o-I Substrates fabricated by Direct Wafer Bonding on Si


1 IBM Research GmbH Zürich Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland
2 CEA, LETI 17, rue des Martyrs, F-38054 Grenoble, France
3 IBM T.J.Watson Research Center, 1101 Kitchawan Rd., Route 134 Yorktown Heights, NY 10598 USA
Email: euc@zurich.ibm.com

Abstract

This paper reports the first demonstration of 200 mm InGaAs-on-insulator (-o-I) fabricated by direct wafer bonding technique (DWB) with III-V donor wafer epitaxially grown on 200 mm Si wafer. The measured threading dislocation density (TDD) of the In0.53Ga0.47As (InGaAs) active layer does not degrade after bonding and layer transfer. Working pseudo-MOS transistors are demonstrated. The fabrication of thin InGaAs-o-I is achieved, using a 50 nm BOX and InGaAs layer as low as 90 nm.

1. Introduction

As Si-CMOS scaling is becoming increasingly challenging, III-V compound semiconductors such as In0.53Ga0.47As (x≥0.53) (InGaAs) are receiving an increasing interest as channel material for nFET [1,2]. Together with SiGe as a pFET channel, they are considered as potential candidates to replace silicon for low power, high performance CMOS thanks to their better transport properties. A prerequisite for the co-integration with silicon in future CMOS technology nodes is the formation of high quality III-V heterostructures on large scale wafers.

Direct wafer bonding (DWB) is considered as one of the possible paths towards this objective [3]. DWB has been proven as a possible path to obtain InGaAs-o-I structures in blanket films and for devices such as FinFETs or HBTs [7,8]. In this paper, we show that III-V virtual substrates grown on large Si wafers can be used as donor wafers. Due to the large lattice mismatch between Si and InGaAs, the final roughness of the as-grown InGaAs is however not compatible with the DWB process. Using chemical-mechanical-polishing (CMP), low roughness InGaAs grown on Si wafer can be transferred by DWB to a Si receiver wafer via a 50 nm BOX. In addition, thanks to the high bonding energy [9], post-transfer CMP on InGaAs-o-I can be used to reduce its thickness to values compatible with device fabrication.

2. Substrate fabrication

A fabrication path for large size InGaAs-o-I substrate is reported in Figure 1. The donor wafer consists of 500nm Ga(Al)As layer grown by MBE and MOCVD on 200 mm Ge/Si (100) substrate, 6° off oriented towards <111> direction to suppress the formation of antiphase domain. 1.5-2 µm thick metamorphic In0.53A10.47As grading buffer (MB) allows reaching InP lattice-matching conditions. The In-content for MB is linearly graded (x~0-65%), followed by an inverse step layer (x=53%). The formation of a 500nm InGaAs active layer completes the heterostructure. Since the surface roughness of the donor wafer (RMS ≥6.5 nm) does not allow for DWB, CMP is performed directly on the InGaAs layer to smooth the surface down to <0.5nm RMS. DWB of the CMPed InGaAs layer is performed after the deposition of a 30 nm thin Al2O3 BOX by ALD. A 20 nm Al2O3 BOX is also deposited on the 200 mm receiver Si (100) wafer. After wet-cleaning, the donor and receiver wafers are immediately brought into contact and annealed between 200 and 300°C for two hours. Finally, the donor wafer is removed by wet and dry etching, resulting in a 200 mm InGaAs-o-I substrate.
3. Results and discussion

The crystalline quality of the InGaAs layer through the full process is controlled by high-resolution X-ray diffraction (HR-XRD) measurements (Fig. 2). The diffraction peak ~63.5° corresponds to InGaAs and is the only peak remaining after DWB and removal of the donor wafer and heterostructure. The absence of Si peak is due to the 6° misalignment between InGaAs-o-I and the receiver wafer. The FWHM of the rocking curves (RC) of InGaAs on the donor wafer is ~900-1300 arcsec, and remains the same after DWB and transfer, which corresponds to a TDD of low 10^9 cm^2 according to Ayer’s model [10]. The best values reported so far for InGaAs virtual substrates are as low as 10^9 cm^2 [11], comparable to values reported for layers grown by the aspect ratio trapping (ART) method [12]. The picture of a 200 mm InGaAs-o-I substrate is displayed in the inset of Fig. 2.

![AFM surface topography and corresponding roughness of the a) InGaAs after growth, b) after III-V CMP, c) after DWB and transfer, and d) after partial CMP of the transferred layer (further improvement still ongoing). Surface topography is 20 x 7 μm.

The AFM surface roughness of the InGaAs at different stages of the full process is shown in Fig. 3. A tremendous improvement is obtained after the InGaAs CMP step, decreasing roughness from 8 nm RMS down to 0.4 nm. After DWB and transfer, the bottom interface of the as-grown InGaAs becomes the new top surface, whose roughness can also be reduced by a second CMP step (Fig. 3d).

![Cross-sectional STEM micrographs of a) as-grown III-V on silicon and b) InGaAs-o-I after the second CMP step.

The cross-sectional STEM micrographs of the “as grown” heterostructure on Si and of the obtained InGaAs-o-I substrate after DWB are shown in Fig. 4. Thin InGaAs-o-I structure is obtained with 50 nm BOX and 90 nm InGaAs (Fig. 4b). Thinner InGaAs layer should be obtained with this fabrication process and are currently under investigation.

![Transfer (a) and output (b) characteristics of a pseudo-MOSFET based on the InGaAs-o-I substrates (450 nm thick InGaAs).

The current-voltage (I-V) characteristics of our InGaAs-o-I structures were measured on pseudo (Ψ)-MOSFET having etched mesa of variable width and length with patterned tungsten source and drain top electrodes and backside gate. The transfer and output characteristics (Figs. 5a-b) confirm their good structural quality and the absence of high residual doping. The large I_{off} current is due to the rather thick InGaAs layer (t=450 nm) and the difficulty to turn off the channel is due to non-optimal electrostatic control. Thinner InGaAs body (t<100 nm) would solve this problem.

4. Conclusions

We demonstrated the successful fabrication of 200 mm InGaAs-o-I substrates from III-V grown on Si, using DWB process. Very thin InGaAs-o-I with high electron mobility have been achieved, opening the way to large scale production of such advanced substrates for the future technology nodes.

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References