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A New Method to Effectively Separate PBTI-induced Shallow and Deep Energy Traps in a 28nm High-k Metal-Gate MOSFET

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Abstract- An experimental approach has been developed to separate the shallow and deep energy traps in a 28nm high-k and metal gate (HKMG) nMOSFET with Fluorine co-implant. This was achieved by the concept of thermal Frenkel-Poole emission and direct-tunneling. It was shown that, for a weaker PBTI stress, the shallow energy trap(SET) dominates the device degradation, but for a heavier PBTI stress, the deep energy trap(DET) dominates. Results showed that, although F ions can alleviate both types of traps, compared to DET, SET is difficult to be alleviated efficiently. Moreover, after the HC stress, not only the conventional hot electrons contribute to the generation of deep energy trap, but also the cold electrons contribute to shallow energy traps. These results provide us a new thinking about the significance of the mechanism of shallow trap in PBTI stressed HKMG CMOS devices.

1. Introduction

With the further device scaling, the high-k metal gate (HKMG) have been launched beyond 28nm to replace the conventional SiON gate dielectric CMOS and to improve the driving current by aggressive reduction of EOT. However, it aroused more reliability issues by the using of new HK materials, such as HfO_2 [1-2]. Among those reliability issues, Bias temperature instability (BTI) is the dominant one to degrade the performance and lifetime of CMOS devices [3-4]. Most reported results claimed that the deep energy traps near the Fermi level are the main origin of the device degradation after the BTI stress [5-7]. However, *rare has been discussed on the effect of shallow energy traps*. In this paper, it raised our interest to develop an experimental method to separate the shallow energy traps (SET) and deep energy traps (DEP), such that different degradation mechanisms of PBTI stress can be identified. Moreover, this approach is further extended to the hot-carrier (HC) stress on HK nMOSFET, and the results will provide us better understanding on the reliabilities of HK CMOS devices.

2. Device Preparation

To improve the reliability, the standard CMOS process with fluorine(F) co-implanted in HK dielectric was used to passivate the interface traps (Fig. 1a), named as **F-devices.** The calculated EOT of stacked dielectrics is 10.5Å. CMOS devices with W/L= 10um/30nm were used in this work, and the control device without F co-implanted was served as a control sample, named as **non-F devices,** (Fig. 1b). Fig. 2 represents the distribution of F ions in HK and interfacial-layer(IL) [8]. Note that the F ions were accumulated at the interface, which are mainly used to passivate the interface traps.

3. Results and Discussion

A. Methodology in the Extraction of Shallow and Deep Energy Traps After the stress

Fig. 3 shows the design of the experiment to describe how to extract the shallow energy trap (SET) from PBTI-induced V_{th}-shift. Since the shallow trap is close to the conduction-band edge, i.e., those type of traps could be emitted easily by raising the environment temperature through the Frenkel-Poole(F-P) emission, the experiment is designed to gradually emit SET by ramping the temperature step by step during the recovery stage after the PBTI stress. Then, by applying the F-P equations, a simple formula can be derived, Table 1:

$$N_o = C\Delta V_{th}(t)\, e^{P(i)t}/q \qquad (1)$$

where t is the recovery time, a function of temperature, and N_o is trap density for each shallow energy level; P is the de-trapping probability representing the emission rate of F-P process,which can be fitted from the experimental data. By utilizing this method, the results are exhibited in Fig. 4. After the PBTI stress, the V_{th} is ramped up to a higher value, i.e., 0.09V, then, during the following recovery process, electrons can be pulled out from the trap by the changes of temperature. In order to extract the deep level traps, it should be extracted from the fresh devices before any stress, Fig. 5. Also, Fig. 6 shows the comparison of the decreasing rate of V_{th} with different temperatures. By fitting the raw data in Fig. 6 with Eq. (1), the trap density of each shallow energy level can be determined, Fig. 7. Furthermore, to separate the SET and deep energy level (DET), in the last stage of the recovery process, a negative bias is applied to de-trap those DET's which are located close to the Fermi-level by the direct-tunneling. From the V_{th} shift after this step, the trap-density of DET can be determined as well, Fig. 8.

B. The Impact of Shallow-energy-trap After the PBTI stress

Figure 9 shows the results of *PBTI test at V_{gs}= 1.5V* and the recovery process. It was found that F-device shows smaller deterioration than non-F one, which means F ions does passivate traps effectively. But what kind of trap is it? After SET recovery stage, F-devices show less amount recovered to non-F devices. On the other hand, during the final DET recovery stage, DET recovery of F-devices is larger than that of non-F devices, and thus F ions passivate mainly SET rather than DET. But, it is worthy to note that the component of SET is larger than that of DET, more than 50% in both device splits. Therefore, the V_{th}-shift of F-devices shows better improvement. Fig. 10 shows a narrow distribution of SET near the conduction band edge from 0.18eV to 0.24eV extracted from Fig. 9. Since SET possesses larger than a half of total traps, the distribution of PBTI-induced traps is reasonably assumed as the peaks appears at the top and bottom; the valley happens in the middle along with the energy in the band-diagram. Fig. 11 shows the results of *PBTI test at V_{gs}= 2V*. Although F-devices show smaller DET, the PBTI-induced V_{th} shift of F-devices is still slightly higher than non-F devices, which is because SET of F-devices cannot be alleviated efficiently and degrades V_{th} in heavily stressed PBTI. Furthermore, in comparison to a *weaker stress in Fig. 9*, Fig. 12(a) shows the stress-recovery results under HC stress. It was found that, after HC, V_{th} of both devices recovers depending on the temperature, which is due to the cold electron injection from the source of channel into the SET position, Fig. 12(b). *In short,* for a *weaker PBTI stress*, the shallow energy trap dominates the device degradation, Fig. 9, but for a *heavier PBTI stress*, Fig. 11, the deep energy trap dominates.

In conclusion, a novel measurement technique has been developed to extract the shallow energy trap (SET) which can be separated from the deep energy trap (DET) after the PBTI stress. It was demonstrated on F-passivated devices. Results show that F can passivate DET efficiently, but not SET, i.e., the V_{th}-shift of F-passivation shows benefits at low V_{gs} (=1.5V) PBTI stress but ineffective at high V_{gs}(2V). It reveals that SET played an important role when BTI reliability is taken into account in HK CMOS devices.

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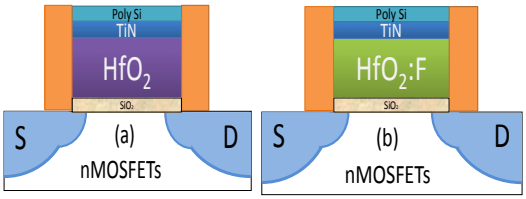

Fig. 1 (a) HKMG nMOSFET made by gate last process. (b) HKMG nMOSFETs by gate last process with HfO_2 dielectric co-implanted Fluorine ions .

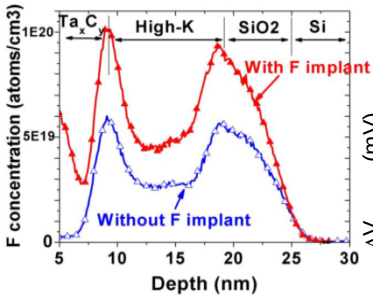

Fig. 2 The distributions of Fluorine in HfO_2 dielectric layer with- and without-Fluorine incorporation. [8]

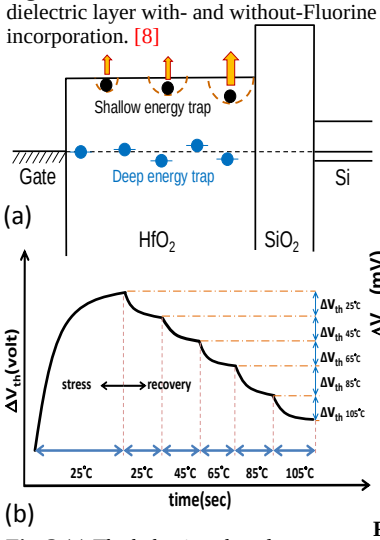

Fig. 3 (a) The behavior that electrons are emitted from trap via Frenkel-Poole emission during the recovery stage. (b) The experiment setup by gradually increasing the temperature to de-trap the electrons during recovery stage.

detrapping rate:

$$\frac{\partial N_{rec}}{\partial t} = -P \cdot N_{rec}$$

$$N_{rec} = N_0 e^{-P \cdot t},$$

detrapping probability:

$$\Delta V_{th}(\text{time}) = \frac{\Delta Q_{rec}}{C} = q\frac{N_0 e^{-P \cdot t}}{C}$$

$$N_{0=} \frac{C}{q} \cdot \Delta V_{th} e^{P \cdot t} \quad ...(1)$$

Table 1 By applying equations of Frenkel-Poole emission **,** a simple equation, (1), can be derived to model the relative energy level of PBTI-induced traps and to extract the trap density at each energy level . Moreover, the energy level is assumed to be the thermal electrostatic , kT, since during the recovery stage, device was kept grounded and with varying environment temperatures.

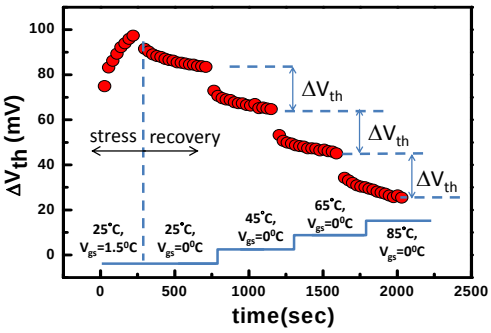

Fig. 4 The experimental results show the V_{th}–shift during recovery stage with varying temperatures.

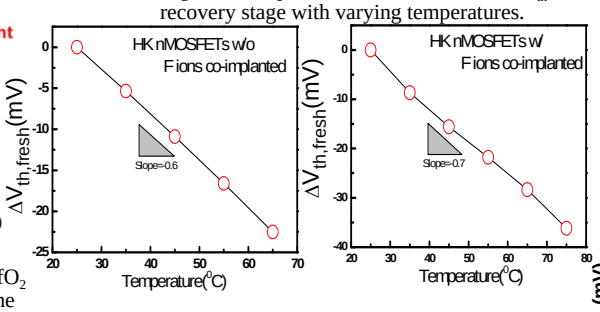

Fig. 5 (a) The V_{th}-shift versus temperature of fresh HK nMOSFETs without F ions co-implant. (b) The V_{th}-shift versus temperature of fresh HK nMOSFETs with F ions co-implant.

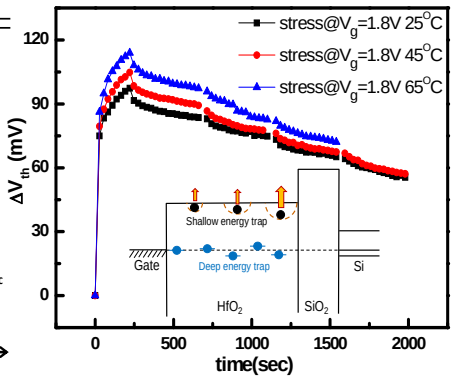

Fig. 6 The experimental results of the recovery process to extract the trap energy level by varying temperatures after PBTI stressed HK-nMOSFETs. (***insert***) The band-diagram to describe the de-trapping process of shallow traps during the recovery.

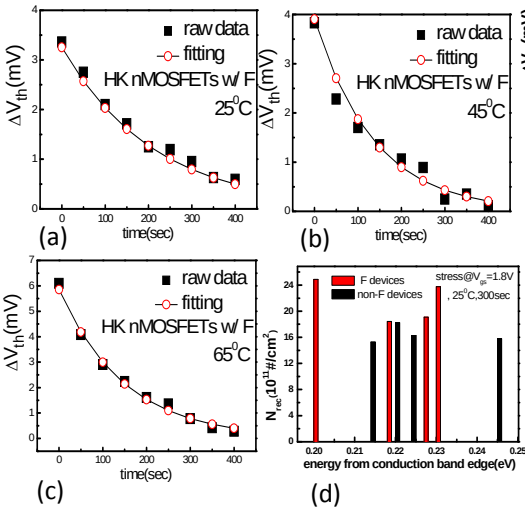

Fig. 7 (a)-(c) The fitting of measured results and the model in 25°C, 45°C, and 65°C respectively for the de-trapping process in the recovery stage, which shows good matches, and Frenkel-Poole emission is a dominant process. **(d) T**he experimental results of the trap density at each shallow energy level.

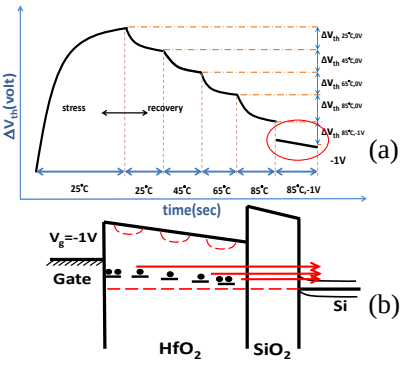

Fig. 8 (a) Different from the previous experimental setup, leaving the device with gate grounded and by varying the temperature only to de-trap after PBTI stress, (b) a negative bias applied on the gate which allows the deep traps to be de-trapped by direct-tunneling through the gate dielectric.

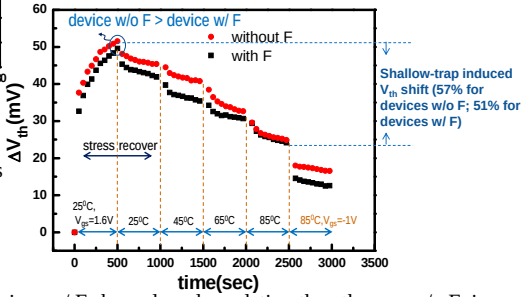

Fig. 9 The devices w/ F shows less degradation than the one w/o F, i.e., F ions serve as a good passivation of shallow energy traps. Moreover, the shallow energy traps are the dominant component (>50%)of total traps, compared to the deep energy traps. Finally, after the recovery of deep energy traps, the Vth shift of device w/o F is also smaller than that w/ F, which further proves that the F ions alleviate the deep-level traps.

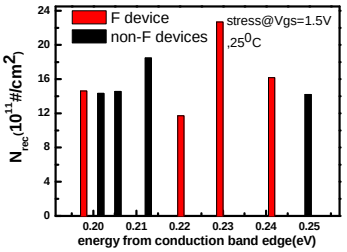

Fig. 10 Several energy levels of shallow traps detected during 0.18eV to 0.24eV from the conduction edge, a narrow distribution. The total trap density of F-device is 5.85#/cm²; that for non-F devices is 6.1#.cm², showing that F co-implant did not alleviate the traps near the conduction band.

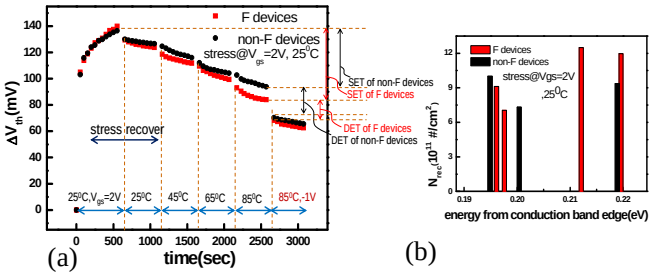

Fig. 11 (a) The experimental results of the recovery process after PBTI stress at Vgs= 2V. Although much smaller recovery of DET for F-device is observed, the PBTI-induced Vth shift of F-devices is slightly larger than that of non-F devices, which is because SET of F-devices cannot be efficiently alleviated by F ions.

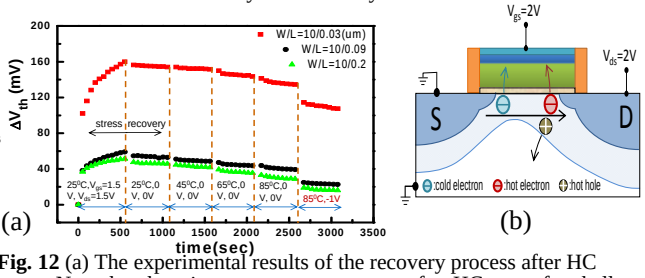

Fig. 12 (a) The experimental results of the recovery process after HC stress. Note that there is recovery process even after HC stress for shallow energy level of traps (b) During HCI stress, not only hot electron injection contributes to the degradation but also cold electron injection does.