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Quantitative evaluation of slow traps near Ge MOS interfaces by using time response of MOS capacitance

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Abstract **We propose a new evaluation method of slow traps near Ge MOS interfaces by utilizing the time response of capacitance in Ge MOS capacitors and evaluate the density and the time constant of slow traps. The slow trap density of the n-Ge MOS capacitor is found to be much larger than that of the p-Ge MOS capacitor, meaning that the higher density of slow traps exist near the conduction band edge.**

1. Introduction Ge has been attracting a lot of interests as one of MOS channel materials because of its higher electron and hole mobility than Si. Here, the realization of the superior Ge gate stacks has been one of the most critical problems for Ge MOSFETs due to the unstable Ge MOS interfaces. Recently, we have proposed an $Al_2O_3/GeO_x/Ge$ gate stack satisfying both thin EOT and low interface state density (D_{it}) by using electron cyclotron resonance (ECR) plasma post oxidation [1]. High electron and hole mobility Ge MOSFETs with this MOS gate stack have been demonstrated under EOT less than 1 nm [2, 3]. However, one of the most serious remaining problems is the gate oxide reliability, typically seen in the time-dependent change of the drain current and the threshold voltage [4, 5]. This time dependence is attributable to slow traps near the Ge MOS interfaces, as shown in Fig. 1. However, the physical characteristics of the slow traps are not clear. The establishment of the quantitative evaluation method of the slow traps is of paramount importance for better understanding of the physical properties.

In this study, we propose a new evaluation method of slow traps near Ge MOS interfaces by utilizing the time response of capacitance in Ge MOS capacitors and evaluate the density and the time constant of slow traps. Also, the impact of post deposition annealing (PDA) in different ambient is examined on the properties of slow traps because the interface states inside the conduction band of Ge have been reported to decrease by PDA in atomic deuterium (D) ambient [6].

2. Experiments Fig. 2 shows the schematic process flow of the $Al_2O_3/GeO_x/Ge$ MOS capacitors. After pre-cleaning of Ge wafers, Al_2O_3(1.4 nm)/GeO_x(0.3 nm)/Ge gate stacks were formed by 1st ALD Al_2O_3 with ECR plasma post oxidation and 2nd-ALD of 1-nm-thick Al_2O_3. PDA was carried out at 400 ºC for 30 minutes in N_2 as the standard condition. PDA in different ambient of H_2, atomic H, D_2 and atomic D was also carried out in order to study the impact of the ambient atmosphere on slow traps. The atomic H and D were generated by cracking H_2 and D_2, respectively, through heated W filaments. Au gate metal and Al back contact were deposited by thermal evaporation.

Fig. 3 shows schematic diagram showing the proposed evaluation method based on *C-t* measurements. In the measurement, V_{trap} is applied first for a given time (T_{trap}) to fill charges into slow states near Ge MOS interfaces. After filling charges, the gate voltage is switched from V_{trap} to a given measuring voltage (V_{hold}) around V_{FB}, where the capacitance change with V_g is large, and the *C-t* characteristics are measured with keeping V_{hold}. The capacitance value at each time is converted into the surface potential and resulting the change in MOS interface charges on an assumption that all the trapped charges locate at MOS interfaces, leading to the measured time response of the MOS interface charges.

3. Results and Discussion Fig. 4 shows the *C-V* characteristics of Au/Al_2O_3/GeO_x/ Ge MOS capacitors. The well-behaved *C-V* curves have been confirmed, though the hysteresis is observed. Fig. 5 shows the measured *C-t* characteristics of Au/Al_2O_3/GeO_x/ Ge MOS capacitors. The capacitance change during the measurement time becomes larger with stronger accumulation bias conditions. It is found that the capacitance in the n-Ge MOS capacitor increases with passing time, meaning that trapped electrons are de-trapping. Also, the larger capacitance change with increasing V_{trap} indicates that the amount of trapped electrons increases with V_{trap}. The capacitance change in p-Ge is, on the other hand, found to be much smaller than that of the n-Ge MOS capacitor. Also, the complicated capacitance transient behavior that the capacitance decreases first and slight increases later is observed. Although this behavior could suggest the co-existence of hole traps and some species in oxides causing ion drift, the physical origin is not clear at present.

Fig. 6(a) and (b) shows the slow trap density and the time constant of the response, respectively. Here, these values in the p-Ge MOS capacitor have been determined as the effective ones from the initial capacitance decrease region, thought the physical origin has not been clear yet. The slow trap density of the n-Ge MOS capacitor is found to be much larger than that of the p-Ge MOS capacitor, meaning that the higher density of slow traps exist near the conduction band edge. Also, the time constant of traps near the conduction band edge is much longer. It is found that the slow traps near the conduction band edge are away from Ge MOS interfaces. Fig. 7(a) and (b) show the amount of slow traps and the time constant in n-Ge, respectively, as a function of T_{trap}. The longer T_{trap} leads to larger amounts of traps and the longer time constant, indicating that the slow traps are distributing from MOS interfaces to the deep inside of the insulators. Fig. 8(a) shows the amount of the slow traps as a parameter of V_{trap}. The stronger accumulation of n-Ge surfaces also provides larger amount of the slow traps, suggesting that the slow traps can widely distribute over both the energy and the distance from the MOS interface, as shown in Fig. 8(b).

Fig. 9(a) and (b) show the impact of annealing in

different ambient on the amount of slow traps and time constant, respectively, in n-Ge. It is found that the annealing is not effective in changing the properties of the slow traps, though the amount of the slow traps seems to slightly increase by PDA in H_2 ambient.

4. Conclusions We have proposed the quantitative evaluation method of slow traps near Ge MOS interfaces by using time response of MOS capacitance and have evaluated the amount of slow traps. It has been found that the Ge MOS interfaces have higher density of slow traps near the conduction band edge.

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References [1] R. Zhang *et al.*, APL **98**, 112902 (2011) [2] R. Zhang *et al.*, TED **59**, 335 (2012) [3] R. Zhang *et al.*, TED **60**, 416 (2014) [4] R. Zhang, *et al.*, IEDM, 642 (2011) [5] J. Franco *et al.*, IEDM, 397 (2013) [6] R. Zhang *et al.*, VLSI symp., T26 (2013).

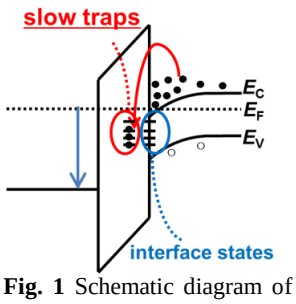

Fig. 1 Schematic diagram of slow traps and interface states

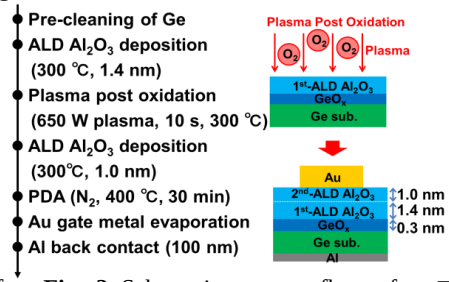

Fig. 2 Schematic process flow of $Au/Al_2O_3/GeO_x/Ge$ MOS capacitor

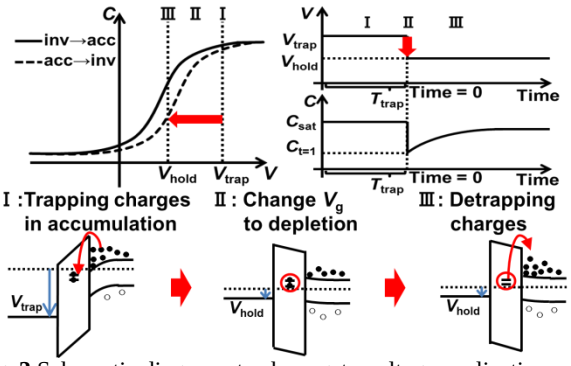

Fig. 3 Schematic diagrams to show gate voltage application in measurements of time response of MOS capacitance

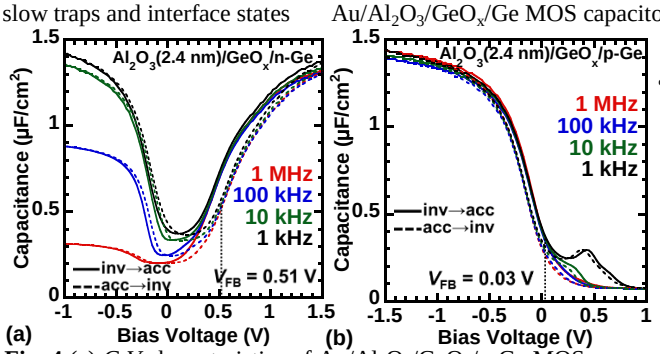

Fig. 4 (a) *C-V* characteristics of $Au/Al_2O_3/GeO_x$/n-Ge MOS capacitor (b) *C-V* characteristics of $Au/Al_2O_3/GeO_x$/p-Ge MOS capacitor

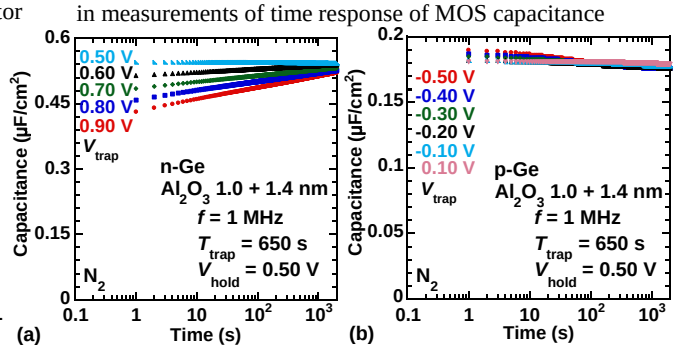

Fig. 5 (a) *C-t* characteristics of $Au/Al_2O_3/GeO_x$/n-Ge MOS capacitor (b) *C-t* characteristics of $Au/Al_2O_3/GeO_x$/p-Ge MOS capacitor

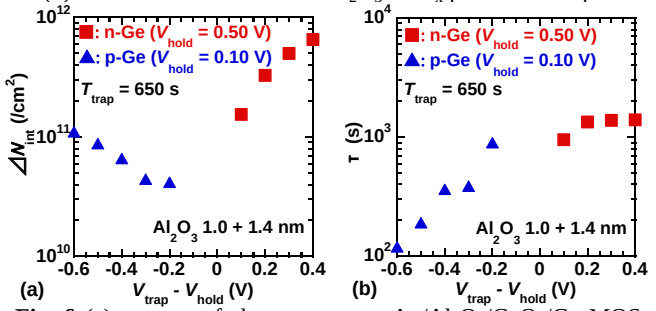

Fig. 6 (a) amount of slow traps near $Au/Al_2O_3/GeO_x/Ge$ MOS interfaces (b) time constant of slow traps near $Au/Al_2O_3/GeO_x/Ge$ MOS interfaces

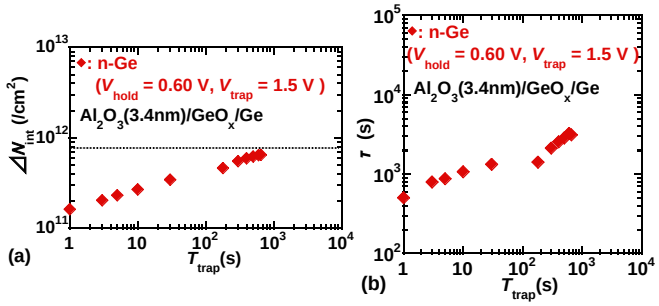

Fig. 7 (a) amount of slow traps near $Au/Al_2O_3/GeO_x/Ge$ MOS interfaces depending on T_{trap} (b) time constant of slow traps near $Au/Al_2O_3/GeO_x/Ge$ MOS interfaces depending on T_{trap}

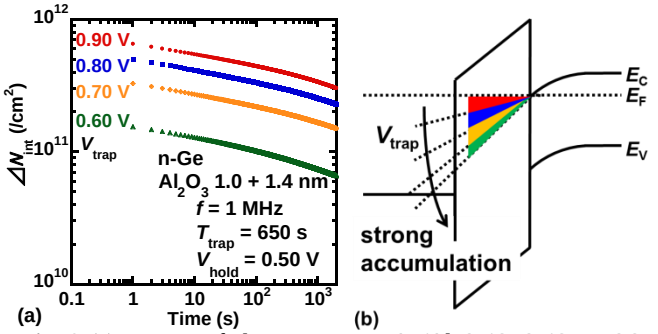

Fig. 8 (a) amount of slow traps near $Au/Al_2O_3/GeO_x/Ge$ MOS interfaces depending on V_{trap} (b) Schematic diagrams of distribution of slow traps depending on V_{trap}

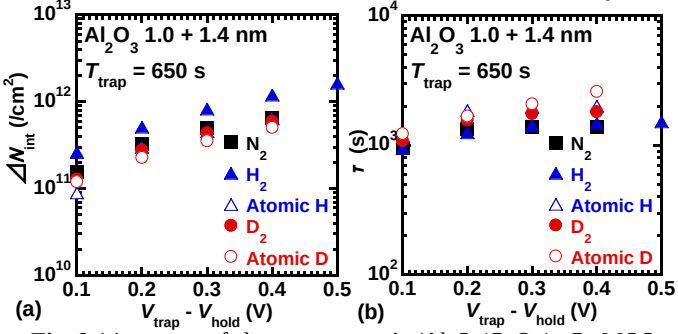

Fig. 9 (a) amount of slow traps near $Au/Al_2O_3/GeO_x$/n-Ge MOS interfaces in different ambient (b) time constant of slow traps near $Au/Al_2O_3/GeO_x$/n-Ge MOS interfaces in different ambient