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Sub-300°C fabrication of poly-GeSn junctionless tri-gate p-FETs enabling sequential 3D integration of CMOS circuits

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Abstract

Poly-$Ge_{1-x}Sn_x$ (x=0~0.08) junctionless (JL) tri-gate p-FETs with L_g of 100 nm and various fin width have been firstly demonstrated blow the processing temperature of 300°C. Major drawbacks in GeSn channel such as junction leakage current due to the bandgap narrowing has been overcome by JL FETs with tri-gate. A very low off current less than 10^{-9} A/μm has been achieved by narrowing of the fin width less than 20 nm for all Sn contents. This leads to superior cut-off characteristics of I_{on}/I_{off} >10^5 at V_d = −50 mV, SS = 125 mV/decades for a Sn content of 3%, which are comparable or better than the counterparts of single-crystalline $Ge_{1-x}Sn_x$ (x = 0 ~ 0.07) p-FETs reported so far. [Keywords: Poly-GeSn, Underwater laser annealing (WLA), Junctionless FET]

1. Introduction

$Ge_{1-x}Sn_x$ on insulator is an attractive channel material for advanced 3D-integrated CMOS circuits (Fig. 1), because it has higher carrier mobilities [1-4] and lower growth temperatures [5,6] than Si and Ge. A technical issue of GeSn channel originates in small bandgap less than 0.66 eV, causing a large junction leakage current, which increase I_{off}. Thus, I_{on}/I_{off} ratio was limited to be 84 [7] or ~5×10^3 [3] even for single-crystalline GeSn planer p-FETs. The JL transistor, which has been proposed by Colinge *et al.* [8] as an alternative to the conventional MOSFETs, is a favorable structure to decrease the I_{off}. The majority carrier transport in heavily doped semiconductor such as Si [8-10] or Ge [10,11] is the key in the JL FETs. It is noted that vacancy and self-interstitial may act as an acceptor [12] in poly-Ge, achieving a heavily doped Ge (typical hole concentration: 10^{18}~10^{19} cm^{-3})[13]. Thus, the JL FET is also good choice for poly-$Ge_{1-x}Sn_x$ devices. In fact, Kamata *et al.* [14] have been recently reported a good cut-off characteristics of I_{on}/I_{off} >10^5 for poly-Ge JL tri-gate FETs, where the crystallization was performed by solid phase crystallization (SPC) at an annealing temperature of 600°C. It is desirable to decrease the polycrystallization temperature further because the temperature is still higher than typical temperature that occurs degradation of the back end of line (BEOL). In our previous study on SPC[5] and WLA[15] of amorphous GeSn (a-GeSn), it was revealed that incorporation of Sn into a-Ge is quite effective to decrease the growth temperature (to 450°C) and enhance the grain size, achieving a relatively high hole mobility (~100 cm^2/Vs).

Under such a background, we report the realization of the world's first *poly*-GeSn JL tri-gate pFETs. The poly-GeSn p-FETs, fabricated using sub-300°C CMOS-comparable process of WLA, exhibit superior cut-off characteristics of I_{on}/I_{off} >10^5 at V_d = −50 mV, SS = 125 mV/decades for a Sn content of 3%, which are comparable or better than the counterparts of *single-crystalline* $Ge_{1-x}Sn_x$ (x = 0 ~ 0.07) p-FETs reported so far.

2. Device fabrication

Key fabrication steps of poly-GeSn JL tri-gate p-FETs are summarized in Fig. 2(a). JL FET fabrication process is greatly simplified, compared to standard MOSFETs one since there are no doping concentration gradients in the device. It should be noted that there are no doping processes in this study. A 60-nm-thick a-$Ge_{1-x}Sn_x$ layer with various Sn content was deposited on SiO_2 layer by sputtering. These a-$Ge_{1-x}Sn_x$ layers were crystallized using a 55-ns KrF excimer laser (wavelength: 248 nm) and were irradiated in flowing water without thermally damaging the underlying substrates [15]. Poly-GeSn fins were formed by e-beam lithography, reactive ion etching (RIE) process (Fig. 2(b)). HfAlO films were deposited as the gate insulator by ALD. TaN metal gate electrodes were deposited by sputtering and patterned by e-beam lithography and RIE process. Self aligned NiGeSn source/drain were formed by annealing at 250°C. Finally, BEOL process was performed at 300°C (Fig. 2(c)). Note that the maximum substrate temperature is limited by BEOL process, not the crystallization process by WLA.

3. Results and discussions

Typical Raman spectra of the $Ge_{1-x}Sn_x$ layers after WLA at ~160 mJ/cm^2 are summarized in Fig. 3(a). Sharp peaks associated with the Ge-Ge vibration mode were clearly observed for all samples. The peak position for the Ge layer is shifted (by ~3.8 cm^{-1}) to a lower wave number than that for the bulk Ge wafer (300 cm^{-1}). This can be attributed to the internal tensile strain in the crystallized grains. Moreover, the peak position for the $Ge_{1-x}Sn_x$ layer is shifted to an even lower wave number than that of the Ge layers, indicating that Sn atoms exist at substitutional sites (Fig. 3(b)).

Electrical properties of the poly-$Ge_{1-x}Sn_x$ layer extracted from Hall measurements were summarized in Fig. 4. Although there was no intentional impurity doping, all samples were *p*-type conduction. The hole concentration for WLA sample was kept as high as about 10^{19} cm^{-3} even for higher Sn content, resulting in better Hall mobility of ~35 cm^2/Vs at x=0.03 compared with SPC sample (~18 cm^2/Vs). We recently reported that holes were generated in epitaxial $Ge_{1-x}Sn_x$ layers (x=0~0.058), which were grown on SOI by using MBE [2]. The hole concentration increased with the Sn content and reached to high values (3×10^{18} cm^{-3}) at x=0.058 and its mobility was ~100 cm^2/Vs at 300 K. Taking the crystallinity that is poly crystal instead of single crystal into consideration, the decrease in the mobility is reasonable.

FET characteristics for WLA sample with x=0.03 were shown in Fig. 5. This clearly shows that fin width (W) of 39 nm is insufficient for cutting off the channel, whereas W less than 28 nm is effective for squeezing the channel. In particular, a large I_{on}/I_{off} ratio of 1.4×10^5 and good I_d-V_d characteristic were obtained in the JL FET with W of 17 nm. A very low I_{off} less than 10^{-9} A/μm was achieved by W narrowing less than 20 nm for all Sn contents, resulting in increase of the I_{on}/I_{off} ratio (Fig. 6). It is also found that the subthreshold slope (SS) was decreased with W narrowing (Fig. 7). Interestingly, it is found that better cut-off characteristics were obtained for higher Sn content as shown in Figs. 6 and 7. We speculate that the substitutional Sn atoms have a role to disable some leakage pass. For precise extraction of effective hole mobility, the C_{gc} was measured by split C-V method (Fig. 8). Since the dispersion of C_{gc} in accumulation is small, the frequency of 1 MHz was used. The effective hole mobility of ~31 cm^2/Vs was obtained in the $Ge_{0.97}Sn_{0.03}$ FET, which was comparable to the Hall mobility (~35 cm^2/Vs). Thus, it is expected that further enhancement of the mobility by improvement of the crystal quality of the poly-GeSn layers. Finally, we show the comparison of our poly-$Ge_{1-x}Sn_x$ JL tri-gate p-FET with the previously reported $Ge_{1-x}Sn_x$ MOSFET works (Fig. 9). The obtained I_{on}/I_{off} and SS in this work are comparable or better than the counterparts of *single-crystalline* $Ge_{1-x}Sn_x$ (x = 0~0.07) p-FETs reported so far.

4. Conclusions

We report the first demonstration of poly-GeSn JL tri-gate p-FETs. Key highlight of this work also include sub-300°C polycrystallization method of WLA and an implant-less FET fabrication process. Recorded cut-off characteristics of poly-$Ge_{0.97}Sn_{0.03}$ tri-gate p-FETs with I_{on}/I_{off} >10^5 at V_d=−50 mV and SS=125 mV/decade have been successively realized by thinning the fin width down to around 20 nm. These results are quite informative for realizing sequential integration of poly-GeSn FETs in a 3D-IC without degradation underlying circuits.

Acknowledgements

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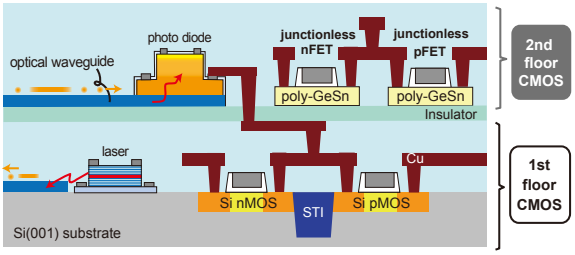

Fig. 1 A schematic illustration of next-generation 3D-IC. The 2nd floor CMOS should be fabricated at a low-temperature process under 450°C to prevent degradation of BEOL and 1st floor CMOS.

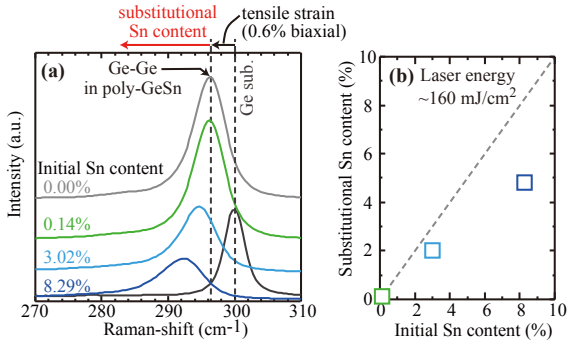

Fig. 3 (a) Raman spectra obtained from poly-GeSn layers with various Sn content after WLA at E~160 mJ/cm^2. (b) Corresponding substitutional Sn content estimated from (a). The decrease at large Sn content redion means the Sn precipitation in the grains.

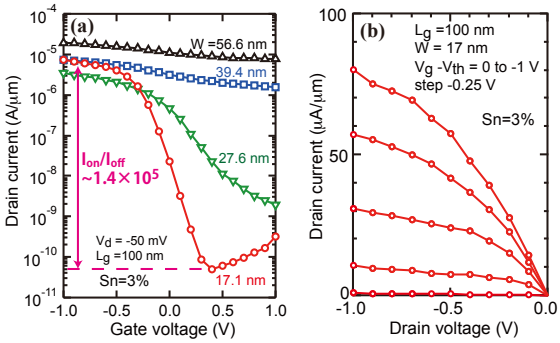

Fig. 5 (a) Vg-I$_d$ and (b) V$_d$-I$_d$ characteristics for Sn=3%.

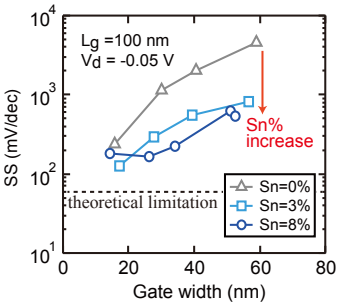

Fig. 7 SS as a function of gate width for various Sn contents. A good SS of ~125 mV/dec is obtained for Sn=3% with the gate width of ~17 nm.

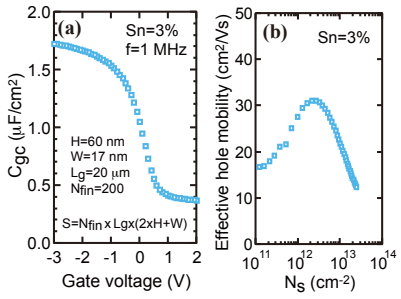

Fig. 8 (a) Split C-V curve of a multi fin FET with the Sn=3% measured at a frequency of 1 MHz. (b) Effective hole mobility extracted from (a). The peak mobility of ~31 cm^2/Vs was comparable to Hall hole mobility shown in Fig. 4(b).

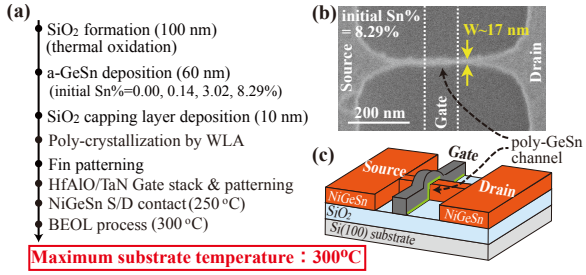

Fig. 2 (a) Key process steps used in the fabrication of poly-GeSn JL tri-gate *p*-FETs, where the maximum substrate temperature was 300°C (BEOL). (b) Top-view SEM image of a poly-GeSn after fin patterning and (c) schematic of a completed poly-GeSn JL tri-gate fin FET. The poly-crystallization were performed by using underwater laser annealing (WLA), which is very useful for low-temperature growth of Ge-rich GeSn [Kurosawa et al., APL **104**, 061901 (2014)].

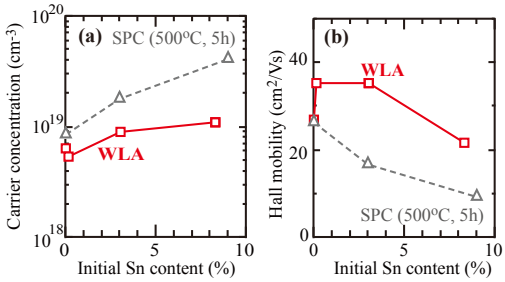

Fig. 4 (a) Carrier concentration and (b) Hall mobility in poly-GeSn layers of 60 nm after WLA at E~160 mJ/cm^2 extracted from Hall measurements. Carrier type is *p*-type for all samples.

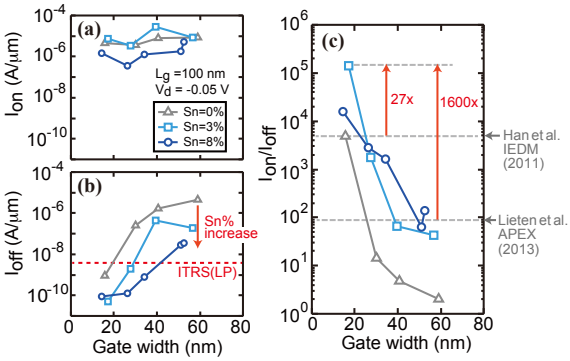

Fig. 6 (a) I$_{on}$, (b) I$_{off}$, and (c) I$_{on}$/I$_{off}$ as a function of gate width for various Sn contents.

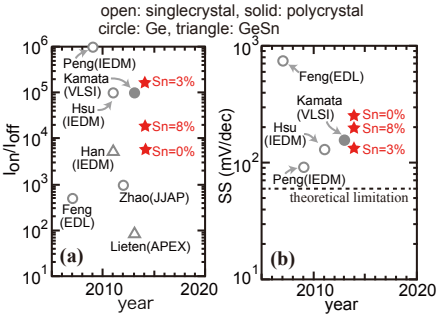

Fig. 9 (a) I$_{on}$/I$_{off}$ and (b) SS in single- and poly-Ge multi-gate FET and single-GeSn planer FET with a calendar year. Red stars are by our group, grey symbols are by others in literatures. The obtained values in this study are outperforming that for single-GeSn and comparable with single-Ge.