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Reduction of Defect State Density at SiO_2/SiC Interface Formed by the Thermal Oxidation Accompanied with Direct CO Generation

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Abstract

Successful annihilation of interface defects at SiO_2/SiC interface through the control of oxidation processes was demonstrated. Capacitance-voltage and conductance measurements were employed at 150 – 300 K to investigate the energetic distribution of the interface defect state density.

1. Introduction

Thermal oxidation of SiC has been reported to induce high density of defects at the interface of SiO_2/SiC. Since the carbon residues are the most possible origin of those defects[1], it is crucial to employ oxidation conditions suitable for the elimination of carbon-related byproducts from the interface.

2. Kinetic and Thermodynamic Considerations

From the kinetic viewpoint, it would be beneficial to limit the oxide thickness to enhance CO out-diffusion. We have reported that the thickness region ~15 nm is thin enough for the interface-reaction-limited growth for the dry oxidation at 1100 – 1300°C on 4H-SiC (0001) [2]. From the thermodynamic viewpoint, we need to select the oxidation temperature and the O_2 partial pressure (pO_2) suitable for the enhancement of CO ejection. For the ideal case, the SiO_2 formation is accompanied with the direct formation of CO molecule from SiC. Based on a thermodynamic model [3], three distinct reactions are estimated to be dominant depending on oxidation temperature and pO_2, as shown in Fig. 1 (a). It is noticed that the ideal reaction ($SiC + 3/2O_2 \rightarrow SiO_2 + CO$) occurs only in the limited range of temperature for a given pO_2. Taking into account the solubility limit of O_2 in SiO_2 [4], the effective pO_2 at SiO_2/SiC interface is calculated to be ~5×10^2 Pa for a oxidation in 1-atm O_2 ambient. Then the temperature window for the ideal reaction in 1-atm pO_2 is estimated to be 1100 – 1400°C. To clarify the transition temperature between ideal and carbon-precipitation ($SiC + O_2 \rightarrow SiO_2 + C$) reactions, activation energies of interface reactions were investigated. First, oxide growth rates were determined from the slopes as observed in the inset of Fig. 1 (b), which shows oxidation time dependence of SiO_2 film thickness. Then, from temperature dependence of oxide growth rates, activation energies of interface reactions were obtained. As shown in Fig. 1 (b), transition of interface reactions was observed at ~ 1070°C, which is close to the thermodynamic prediction.

3. Electrical properties of SiC-MOS capacitors

(1) Nearly-ideal capacitance-voltage characteristics

4H-SiC (0001), Si face, wafers with ~1×10^{16} cm^{-3} doped n-type epitaxial layers were cleaned in diluted HF, followed by the oxidation at 1300°C in 1-atm dry O_2 with the ramp-heating furnace. A short rise/fall time (>600°C/min) was employed to minimize the unwanted additional oxidation at lower temperature where the carbon precipitation would be more pronounced. After the growth, some films were annealed additionally at 800°C in O_2 for 30 min aiming for the annihilation of oxygen vacancies [5]. Note that 800°C is sufficiently low temperature to neglect the additional oxide growth in 30 min.

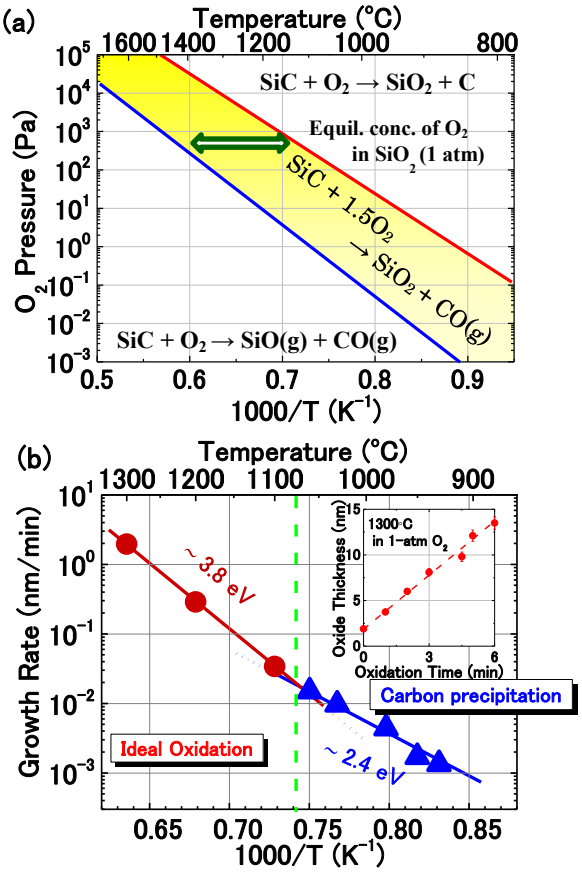

Fig. 1 (a) Temperature-pO_2 phase diagram for the reaction between surface SiC and O_2. (b) Arrhenius plot of oxide growth rate. The inset shows the oxidation time dependence of SiO_2 film thickness grown on 4H-SiC (0001) at 1300°C.

The bidirectional capacitance-voltage (C-V) characteristics measured with various frequencies from 1 kHz to 1 MHz are shown in Fig. 1. Not only the hysteresis but also the frequency dispersion of the C-V curve is well suppressed except for the depletion region where the effects of interface states appear slightly. The good agreement of the

C-V curves with the ideal curve calculated from Poisson's equation, shown as a broken line in Fig. 1, indicates the formation of the interface with low defect state density.

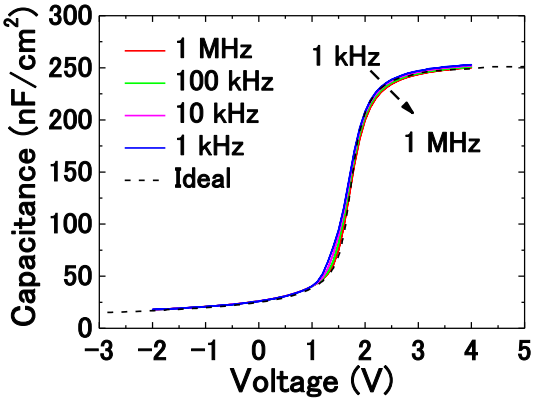

Fig. 2 Bidirectional C-V characteristics of the MOS capacitor (T_{ox} ~ 14 nm) fabricated by 1300°C oxidation followed by POA at 800°C in O_2. Ni and Au were evaporated as back and gate electrode, respectively. Broken line shows the ideal C-V curve calculated by Poisson's equation.

(2) Effects of defects near the conduction band edge

The interface state density (D_{it}) was estimated by the conductance method. The typical results of frequency dependence of Gp/ω are shown in the inset of Fig. 3. From the peaks D_{it} values were determined and shown in Fig. 3 as a function of energy level below the conduction band of SiC. The measurements were done not only at room temperature, but also at 150 K and 200 K to extend the energy range of the characterization toward the conduction band edge of SiC. As a result, we observed interface state density as low as ~10^{11} $cm^{-2}eV^{-1}$ or less, which are lower than the reported values of as-oxidized films [6]. It should be noted that the best results were demonstrated by the addition of low-temperature POA at 800°C in O_2 where D_{it} <10^{11} $cm^{-2}eV^{-1}$ was attained even 0.1 eV below the conduction band edge of SiC. The oxidation temperature of 1300°C is high enough to avoid the unwanted low-temperature mode as discussed above, whereas it possibly induces oxygen vacancies, since it is suggested from the thermodynamic consideration that 1300°C is close to the higher limit of the temperature range for ideal reaction, where the generation of SiO would be enhanced. Therefore we speculate that the improvement by the low-temperature POA in O_2 should be mainly attributed to the annihilation of oxygen vacancies.

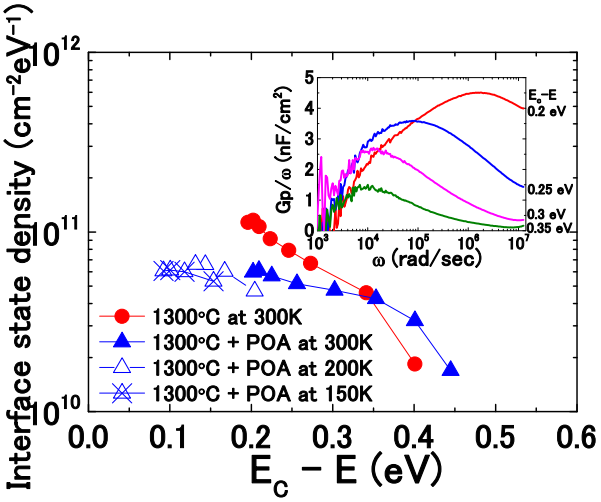

Fig. 3 Interface defect state density as a function of energy level below the conduction band, estimated from the peak values of Gp/ω measured at various temperatures from 150 K – 300 K. The inset shows the frequency dependence of Gp/ω measured at 300 K for the MOS capacitor fabricated by 1300°C oxidation followed by POA at 800°C in O_2.

Although the POA is effective for the removal of interface defects near the conduction band edge, low-temperature C-V measurements revealed that the effects of those defects still exist. High frequency (1 MHz) C-V curves measured at 300 K and 150 K are shown in Fig. 4. It is noticed that the stretch-out of C-V curve is more pronounced at low-temperature measurement. Taking into account that the Fermi energy shifts from 0.19 eV (at 300 K) to 0.084 eV (at 150 K) below the conduction band edge, this result indicates the residuals of non-negligible amount of interface defects at the energy levels of ~0.1 eV from the conduction band edge of SiC even after POA.

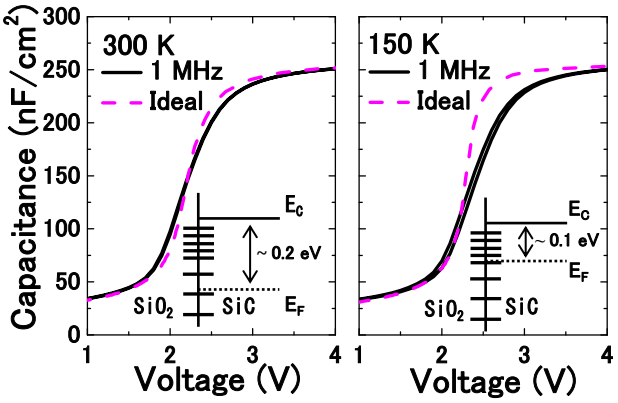

Fig. 4 Temperature dependence of high-frequency (1 MHz) C-V curves measured at 300 K and 150 K for the MOS capacitor fabricated by 1300°C oxidation followed by POA at 800°C in O_2. Broken lines denote the ideal C-V curves.

4. Conclusions

SiC-MOS capacitors with nearly-ideal C-V characteristics were obtained by the control of thermal oxidation. In addition to the employment of suitable oxidation conditions for CO direct ejection mode, POA was revealed to work effectively for a dramatic reduction of D_{it}, especially near the conduction band edge of SiC.

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