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Estimation of real SiC-MOS characteristics by using novel high-speed pulse *IV*

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Abstract

Novel high-speed pulse *IV* successfully estimates real SiC-MOS characteristics while the density of an interface trap is as low as possible. Lateral-MOS characteristics are mainly affected by fast interface traps (< 0.6 μs), whereas trench-MOS characteristics are significantly affected by slow interface traps.

1. Introduction

The progress of developments in SiC power devices is expected to lead to high growth in the power electronics industry. An all-SiC inverter can achieve especially high efficiency [1]. The interfacial state between a channel and gate dielectric in SiC MOS, however, remains poorly understood. According to the latest studies on lateral SiC MOS by using a charge pumping (CP) method, channel mobility is possibly affected by extremely high interface trap density (D_{it}) near the conduction band (E_c) of SiC [2, 3]. On the other hand, nobody has ever observed real SiC-MOS characteristics, which are not affected by the extremely high D_{it}. The present work provides novel high-speed pulse *IV* (HPIV) to demonstrate the SiC-MOS characteristics while D_{it} is as low as possible.

2. Samples and measurement methods

Samples are a lateral MOS and a trench MOS (Fig. 1). Their gate length is 1 μm. The gate dielectric of the lateral MOS is formed on the 4H-SiC (0001) substrate with off-angle of 4°, and that of the trench MOS is formed on trench side walls including the (11-20) face.

Amplitude-sweep CP can identify a time constant (t_c) of interface trap, and HPIV can reduce the influence of the identified interface trap. In a CP sequence and conditions (Fig. 2 and Table I), scanning time (t_{tf}) from threshold voltage to flat band voltage determines observable acceptor-like traps [2]. Measurement with higher t_{tf} can observe shallower interface traps near E_c (Fig. 3). The most important parameters are, therefore, fall time (t_f) and pulse voltage (V_p) which determine t_{tf} (Fig. 2). Figure 4 shows an example HPIV sequence, and table I lists HPIV conditions. In this sequence, waiting time (t_w) before starting drain-current (I_d) measurement determines the amounts of charged traps reducing I_d. When t_w is 0.6 μs, the interface traps with t_c longer than 0.6 μs cannot affect I_d.

3. Increase of I_{cp} due to fast interface traps

Figure 5 shows that charge-pumping current (I_{cp}) depends on t_f. I_{cp} of the lateral MOS at high voltage increases as t_f decreases from 10 to 0.1 μs. Interestingly, when t_f is 10 or 1 μs, saturated I_{cp} of the trench MOS is higher than that of the lateral MOS. SiC dry etching probably creates slow interface traps (SITs) with t_w of about 1 μs. However, as t_f decreases, I_{cp} of the lateral MOS exceeds that of the trench MOS. This feature stands out when t_f are shorter than 1 μs. In our conclusion, the lateral MOS gives extremely high density of fast interface trap (FIT), which is likely to originate in plane orientations, unlike the trench MOS. As summarized in Fig. 6, D_{it} @ 1.37 eV of the lateral MOS (1.5×10^{13} $cm^{-2}eV^{-1}$) is larger than that of the trench MOS (1.0×10^{13} $cm^{-2}eV^{-1}$) because D_{it} near E_c strongly depends on the plane orientations. Furthermore, D_{it} @ 1.25 eV of the trench MOS (2.5×10^{12} $cm^{-2}eV^{-1}$) is larger than that of the lateral MOS (1.6×10^{12} $cm^{-2}eV^{-1}$) because D_{it} near midgap is likely to depend on processes.

4. Demonstration of high-speed pulse *IV*

HPIV can observe dependence of SiC-MOS characteristics on the waiting time (Fig. 7). The change of I_d of the lateral MOS is weak because FITs are fully charged by the time the I_d measurement starts even if t_w is a minimum of 0.6 μs. Trench-MOS data show that I_d rapidly rises when the waiting time is short because I_d is more strongly affected by density of SIT than by density of FIT. Figure 8 demonstrates that I_d shows the exponential decay in the lateral MOS, and I_d is more steeply reduced in the trench MOS than in the lateral MOS. The steep I_d reduction corresponds to G_m degradation from Figs. 8 and 9. Therefore, I_d of the trench MOS is likely to be reduced by not only the density of SIT but also the mobility degradation due to SIT.

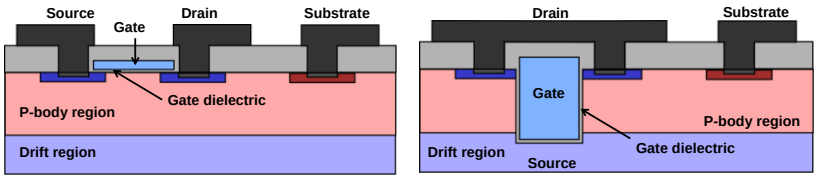
Figure 10 shows dependence of G_m on temperature at t_w = 0.6 μs. In the lateral MOS, G_m at low electric field increases as temperature increases because the mobility is mainly determined by coulomb scattering due to FIT. In the trench MOS, G_m decreases with an increase of temperature because mobility is degraded by the phonon scattering. Figure 11 summarizes the relationship between G_m and temperature. In the trench MOS, a slope of G_m at t_w = 0.6 μs has a negative value slightly larger than that of G_m at t_w = 3 μs because the influence of the coulomb scattering due to SIT increases as t_w increases.

5. Conclusions

HPIV can estimate the real SiC-MOS characteristics while D_{it} reaches a practically low level. As a result, FIT mainly affects I_d in the lateral MOS, and SIT drastically reduces I_d in the trench MOS. SIT has a severe impact on switching characteristics. HPIV helps improve and increases understanding of the interfacial state of SiC MOS.

References

[1] R. A. Wood, and T. E. Salem, T-PE **26** (2011) 2504. [2] D. Okamoto et al., T-ED **55** (2008) 2013. [3] A. Osawa et al, MSF **740-742** (2013) 541.



(a) Lateral SiC MOS. (b) Trench SiC MOS.

Fig. 1 Test structures. Drain is upper electrodes because parasitic capacitance is kept as low as possible in trench SiC MOS.

Table I Conditions.

Conditions of CP

Temperature	27 ºC
Period	100 µs
Rise (t_r) & Fall times (t_f)	0.1, 0.5, 1, 10 µs
Base voltage	-15 V
Pulse voltage (V_p)	-10 ~ 20 V

Conditions of high-speed pulse *IV*

Temperature	25, 75, 125 ºC
Period, Pulse width	100, 50 µs
Rise & Fall times	0.25 µs
Gate voltage (V_g)	0 ~ 10 V
Drain voltage (V_d)	1 V
Waiting time for measurement (t_w)	0.6 ~ 5 µs
Measurement time	10 ns
Source (V_s) & Sub. voltages (V_{sub})	0 V
Gate voltage (V_g)	0 ~ 10 V
Step voltage (V_{step})	0.1 V

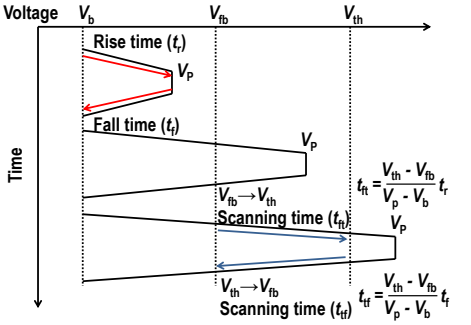


Fig. 2 Amplitude-sweep charge pumping. t_r is the same as t_f.

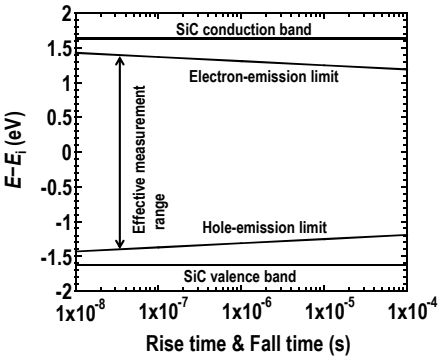


Fig. 3 Relationship between CP parameters and observable traps.

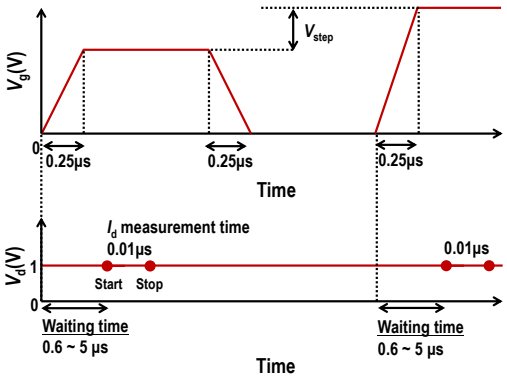
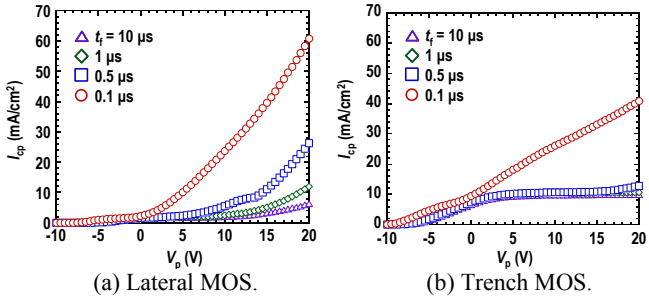
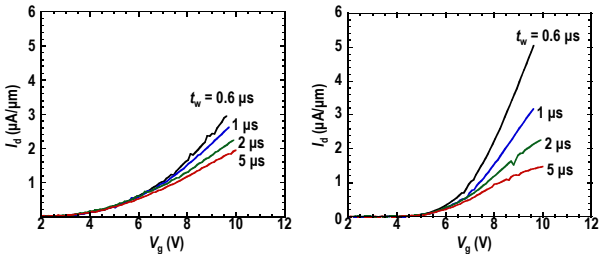


Fig. 4 Sequence of high-speed pulse *IV*. Agilent B1530A was used for high-speed measurement.



(a) Lateral MOS. (b) Trench MOS.

Fig. 5 Dependence of charge-pumping current on t_f.



(a) Lateral MOS. (b) Trench MOS.

Fig. 7 I_dV_g characteristics meaured by high-speed pulse *IV*.

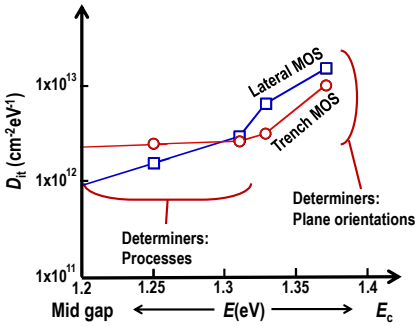


Fig. 6 Difference in D_{it} between lateral MOS and trench MOS. D_{it} is estimated from Figs 3 and 5. In estimation, I_{cp} data @ V_p = 20 V are used.

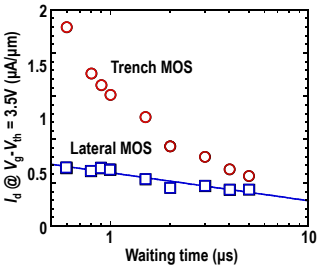


Fig. 8 Dependence of I_d on t_w at 25°C.

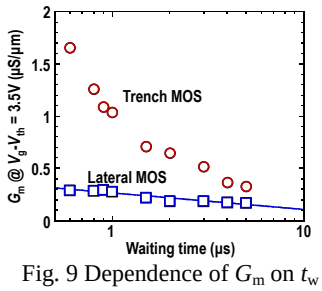
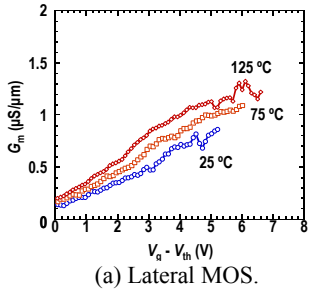
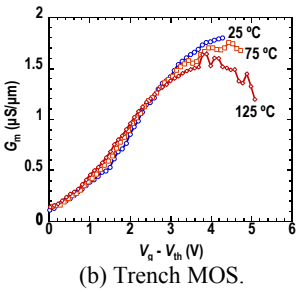


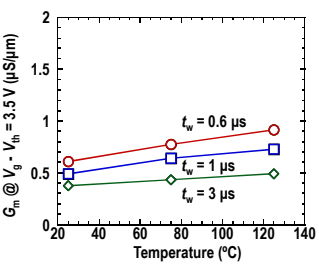
Fig. 9 Dependence of G_m on t_w at 25°C.

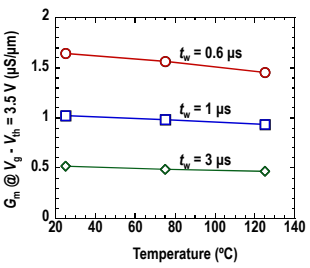




(a) Lateral MOS. (b) Trench MOS.

Fig. 10 Dependence of G_m on measurement temperature. t_w is 0.6 µs.





(a) Lateral MOS. (b) Trench MOS.

Fig. 11 Summary of relationship between G_m and temperature.