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Ultrawideband Ultralow PDN Impedance of Decoupling Capacitor Embedded Interposers Using Narrow Gap Chip Parts Mounting Technology for 3-D Integrated LSI System

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Abstract

We have developed a new chip capacitor embedded interposer using a narrow gap chip parts mounting technology. This interposer is expected to reduce power distribution network (PDN) impedance. As a result, the chip capacitor of 0402 type embedded interposer using the narrow gap chip parts mounting technology shows a low PDN impedance below 0.1 Ω could be evaluated at the frequency range of up to 10 GHz. It can be realized that the PDN impedance of the interposer shows below 1/100 compared with a general interposer with embedded the chip capacitor parts of 0603 types.

1. Introduction

Recently, the three-dimensional (3-D) integrated LSI system, which consists of 3-D stacked LSI chips with through silicon vias, a silicon interposer with thin-film decoupling capacitor, and a decoupling chip capacitor embedded organic interposer on a printed circuit board (PCB), has attracted attention for realizing an advanced high-performance system, as shown in Fig. 1(a) [1]. The system can provide enormous advantages in terms of achieving multifunctional integration, improving the system speed, and reducing power consumption for next-generation LSIs. However, for realizing ultra-high-speed signal processing in a 3-D integrated LSI system, it is necessary to suppress the simultaneous switching noise (SSN) up to a high- frequency range by introducing decoupling capacitor embedded interposers. Such a power distribution network (PDN) provides ultralow PDN impedance, as shown in Fig. 1(b). The required target impedance is determined using the operating voltage and average current drawn by the component. The PDN should have an impedance of less than the target impedance over a frequency range of DC to hundreds of MHz [2]. Therefore, it is required that the high-performance interposers that provide ultralow PDN impedance.

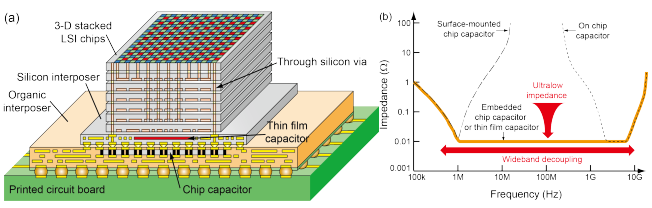


Fig. 1 Schematic of (a) the 3-D integrated LSI system and (b) ultralow-impedance PDN using wideband decoupling capacitor of device embedded interposer for 3-D integrated LSI system.

In this paper, we have developed a new chip capacitor embedded interposer using a narrow gap chip parts mounting technology. It is reported that the interposer test element groups (TEG) were evaluated by using a developed ultralow impedance evaluation system in detail.

2. Capacitor Embedded Interposer Using Narrow Gap Chip Parts Mounting Technology

The silicon interposer is expected in the capacitor embedded interposer where low PDN impedance is achieved by a wide frequency. However, the cost of manufacturing of the silicon interposer that uses semiconductor LSI manufacturing process is very high.

Therefore, we developed a new chip capacitor embedded organic interposer using the narrow gap chip capacitor parts mounting technology. The chip capacitor parts were in a high density embedded interposer by the narrow gap chip parts mounting technology by 0.1 mm at chip capacitor part intervals. The chip capacitor embedded organic interposer with a low PDN impedance enough compared with the silicon interposer was achieved by introducing this chip parts mounting technology. Moreover, it has achieved with high density chip parts mounting technology further by making these chip parts 0402 types. This chip capacitor embedded organic interposer is thought that the manufacturing is lower cost than that of the silicon interposer, cheaper and the product reliability is higher than that of the silicon interposer. We fabricated various types of capacitor embedded interposer TEG, such as the chip capacitor embedded organic interposer using the narrow gap chip parts mounting technology, the general chip capacitor embedded organic interposer, and the thin film capacitor embedded silicon interposer using the same design to verify the mounting method of the decoupling capacitor. The size of this interposer TEG is 20 mm × 20 mm and that of the capacitors mounted area on the interposer is 10 mm × 10 mm, as shown in Fig. 3. The capacitors that show 1.0 - 1.2 μF were mounted on each of these interposer TEGs at a

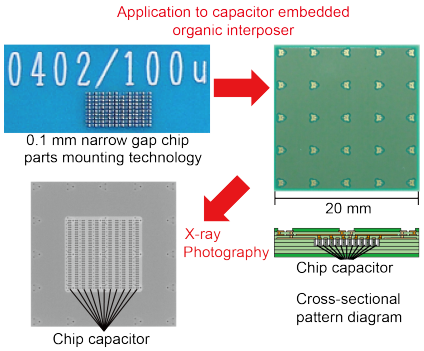
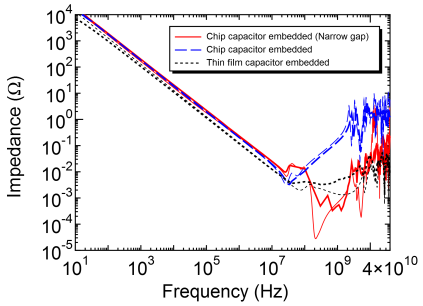


Fig. 3. Photographs, Cross-sectional views, and X-ray photograph of the fabricated capacitor mounted or capacitor embedded organic interposer using the narrow gap chip parts mounting technology.

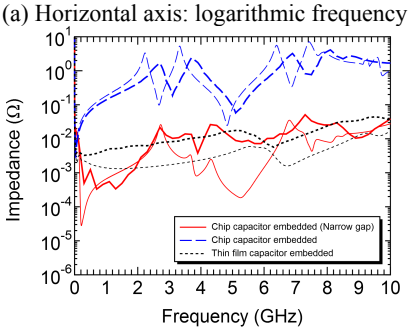
10 mm × 10 mm part. The interposer TEGs have 25 probe pads. 341 chip capacitors of the 0402 (0.4 mm × 0.2 mm) case size are inside the chip capacitor embedded interposer TEG using the narrow gap chip parts mounting technology. For a 0402 chip capacitor, the value is 3.3 nF. Total capacitance value becomes 1.125 μF on the TEG. 48 chip capacitors of 0603 (0.6 mm × 0.3 mm) case size are inside the chip capacitor embedded interposer TEG. For a 0603 case-sized chip capacitor, the value is 22 nF. Total capacitance value becomes 1.056 μF inside the TEG. One $SrTiO_3$ thin film capacitor of 1.2 μF is inside the silicon interposer TEG. Figure 3 shows X-ray photograph of the fabricated chip capacitor embedded organic interposer using narrow gap chip parts mounting technology. 341 chip capacitors seem to be buried inside the organic interposer.

3. Evaluation

We calculated and measured the PDN impedance of the decoupling capacitor embedded interposer TEGs using the developed ultralow impedance evaluation system [3][4]. Because power ground pin generally layout is peripheral assignment on the LSI chip, we evaluated the PDN transfer impedances Z_{21}. Figure 4(a) shows logarithmic plot of the measured PDN transfer impedances Z_{21} are plotted against frequency. Figure 4(b) is plotted again on the basis of Fig. 4(a) with the frequency axis on a linear scale. The calculated results are in good agreement with the measured ones at a wide frequency range. In particular, the interposer TEGs like thin film capacitor embedded interposers that show a low impedance of approximately 0.001 Ω could be evaluated and calculated accurately. Therefore, it is considered that the change in the impedance is caused by the small change in the layout of the chip capacitors, and the difference in the electrode structure of the thin film capacitor using high-k dielectric materials can be evaluated and calculated. These results are thought to be realized precision calculation and measurement of PDN impedance. As a result, the chip capacitor embedded interposer using the narrow gap chip parts mounting technology shows a low PDN impedance below 0.1Ω could be evaluated at the frequency range of up to 10 GHz. This is realized that the interposer shows the comparable level of the PDN impedance as the thin film capacitor embedded silicon interposer. It can be realized that the PDN impedance of the interposer shows below 1/100 compared with a general interposer with embedded the chip capacitor parts of 0603 types.



(a) Horizontal axis: logarithmic frequency



(b) Horizontal axis: linear frequency

Fig. 4 Measured and calculated PDN transfer impedance Z_{21} plotted against frequency against frequency, where the solid line indicates the chip capacitor embedded organic interposer using the narrow gap chip mounting technology, the dashed line indicates the chip capacitor embedded organic interposer, and the dotted line indicates the thin film capacitor embedded silicon interposer. Thick lines indicate measured waveforms. Thin lines indicate calculated waveforms at 2.5-D FEM using the SPICE model as the chip capacitor model. (a) Horizontal axis indicates logarithmic frequency. (b) Horizontal axis indicates linear frequency (Vertical axis: logarithmic PDN impedance.)

4. Conclusions

We have developed a new chip capacitor embedded interposer using a narrow gap chip parts mounting technology. It is conjectured that PDN of the chip capacitor embedded organic interposer using the narrow gap chip parts mounting technology having this impedance value enough to suppress the SSN on the PDN. Therefore, by using the chip capacitor embedded organic interposer using the narrow gap chip mounting technology for 3-D integrated LSI system, it is expected that the PDN of the system can be achieved ultralow PDN impedance.

References

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