Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp720-721

Characterization of Vapor Deposited Polyimides and Process Integration with the Polymeric Liner for Via-Last/Backside-Via Cu-TSV Formation

Takafumi Fukushima, Murugesan Mariappan, Jichoel Bea, Kang-Wook Lee, and Mitsumasa Koyanagi

Global INTegration Initiative (GINTI), New Industry Creation Hatchery Center (NICHe), Tohoku Univ.
6-6-10 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-795-4119, E-mail: fukushima@bmi.niche.tohoku.ac.jp

Abstract A vapor deposited polyimide (PI) as a TSV (through-Si via) dielectric liner is studied for 3D integration based on via-last/backside-via processes. In this work, Kapton-H® is employed for a candidate of the PI TSV liner. The leak current (~ 1×10^{-9} A/cm^2) of the vapor deposited PI is low, and in addition, the PI liner shows lower thermal mechanical stress than a SiO_2 liner deposited by plasma CVD with TEOS. The etching rates of the vapor deposited PI formed on the via top, sidewall, and bottom are approximately 1,300, 400, and 1,000 nm/min, respectively, suggesting that the vapor deposited PIs can be applied to TSV liners for via-last/backside-via 3D integration.

1. Introduction

In 1995, Matsumoto *et al*., have reported the first TSVs that are composed of thermal oxide as a TSV liner and P-doped poly-Si as a conductive material [1]. The poly-Si TSVs formed by LPCVD using the via-first approach were called “Vertical Buried Interconnections” in those days. TSV formation is a key interconnect technology for 3D chip stacking that can provide high-performance and low-power LSI without further scaling down device sizes. More recently, the via-last/backside-via approach has attracted much attention for 3D integration due to high design flexibility, low process complexity/cost, and low entry barrier in manufacturing, compared to the via-middle approach [2]-[4]. SiO_2 have been widely used as TSV liners. The oxide formed by sub-atmospheric CVD with TEOS/O_3 shows high step coverage (>80%) for deep Si vias. However, the deposition temperature is high at above 350°C that gives thermal damage to temporary adhesives. On the other hand, the other oxide formed by plasma CVD with TEOS/O_2 have a great advantage in low deposition temperature at below 200°C, but the step coverage is very low (~20%). Therefore, the deposition of the thick plasma oxide over 1,000 nm on the bottom sidewall of deep Si vias is challenging to obtain low capacitance below 50 fF for 10-μm-diameter TSVs, as shown in Fig. 1. To solve the problems, we employ a vapor deposited PI as a TSV liner [5]. The PI can be conformably formed on deep Si vias with high step coverage over 80% at below 200°C. In the present paper, we characterize vapor deposited Kapton-H® used as a TSV dielectric liner and integrate a process with the polymeric liner for Cu-TSV formation by the via-last/backside-via method.

2. Experimental

Pyromellitic dianhydride (PMDA) and 4,4'-oxydianiline (ODA) were used for vapor deposition of a PI. Fig. 2 shows a schematic illustration of the mechanism for vapor deposition polymerization of the monomers. This technique has characteristics of both PVD and CVD methods. Two kinds of the bifunctional monomers were co-evaporated without carrier gases, and then, the monomers adsorbed onto a Si substrate with deep Si vias. After that, the monomers thermally reacted with the other monomers with surface migration on the substrate to give oligomer or were re-evaporated from the substrate. Finally, the surface reaction progressed on the substrate, resulting in a fully cured polyimide.

3. Results and Discussion

Fig. 3 shows I-V characteristics of two different thin insulating layers. One is 400-nm-thick SiO_2 by plasma CVD with TEOS at 200°C and 385°C, and the other is PI with thicknesses of 500 nm and 1,300 nm by vapor deposition polymerization at 200°C. 1-μm-thick and 0.5-mm-diameter Al electrodes are employed in this measurement. The values of leak current ranged from -20 V to 20 V are below 1×10^{-12} A, indicating that the insulating characteristics of the vapor deposited PI is comparable to the oxide. In addition, the vapor deposited PI exhibits lower thermal/mechanical stress than that of the oxide. Fig. 4 shows cross-sectional stress/strain mapping images of Si between adjacent Cu-TSVs (diameter: 12 μm and depth: ~50 μm). Compared to the TSVs with the oxide liner, tensile stress applied to the wafer surface between the TSVs with the PI liner is large in the vertical and horizontal dimension.

Fig. 5 (a) shows a process flow of Cu-TSV formation based on a via-last/backside-via scheme. First, a thick Si wafer with wirings is temporarily bonded to a support glass wafer in a face-down fashion, and then the Si wafer is thinned form the backside. After that, deep Si vias are formed by Botch process with C_4F_8 and SF_6, followed by TSV liner deposition. The subsequent process is contact etching at the bottom of the vias by mask-less RIE. Thus, etching selectivity of the TSV liner on the top, sidewall, and bottom of the vias is key factor to electrically interconnect between front side and backside wirings through Cu-TSVs. Fig. 5 (b)-(e) shows SEM cross-sectional images of deep Si vias (diameter 30 μm, depth 250 μm, aspect ratio > 8) after via-bottom liner etching with O_2, Ar, and fluorocarbon gases. The etch rate of the via top is 1,320 nm/min, whereas the etch rate of the via bottom is 990 nm/min. On

the other hand, the etch rate of the via sidewall is 400 nm/min. These results suggest that such high etch selectively gives successful contact opening without excess sidewall etching to the Cu-TSV formation.

4. Conclusions

The leak current of vapor deposited Kapton-H® was nearly as low as SiO_2 deposited by plasma CVD. In addition, the PI TSV liner exhibited lower thermo-mechanical tensile stress to surficial Si between Cu-TSVs than the plasma oxide. By controlling etching rates between via top/bottom and via sidewall, PI liners can be utilized to the via-last/backside-via 3D integration processes.

Acknowledgments

This work was supported by JSPS KAKENHI (Multi-year Fund), Grant-in-Aid for Challenging Exploratory Research: Grant Number 25630118.

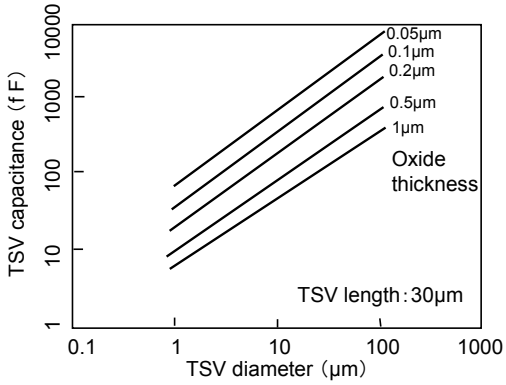

Fig. 1 TSV capacitance as a function of TSV diameter in varying TSV oxide thickness (simulation).

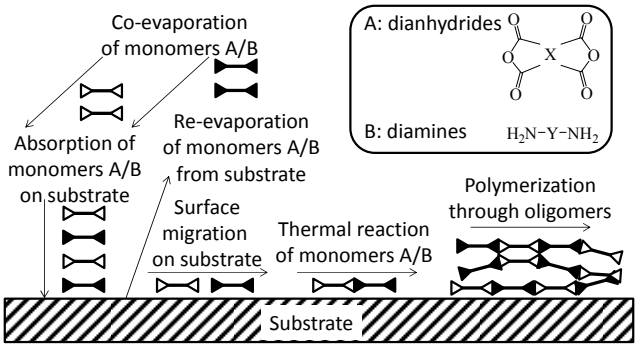

Fig. 2 A schematic illustration of the mechanism for the formation of vapor deposited PIs.

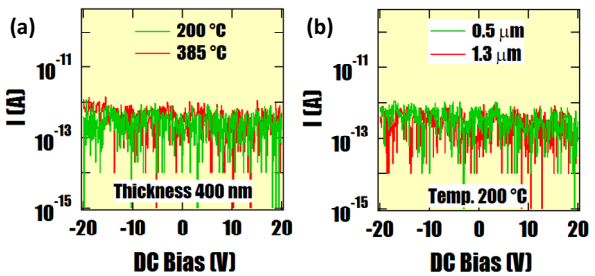

Fig. 3 I-V data of sheet oxide (a) and PI (b) layers.

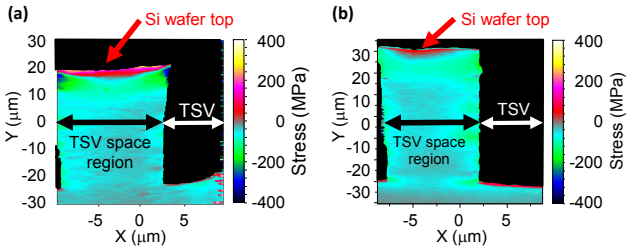

Fig. 4 Cross-sectional mapping on stress/strain of Si between Cu-TSVs by μRaman spectroscopy: oxide (a) and PI (b) liners.

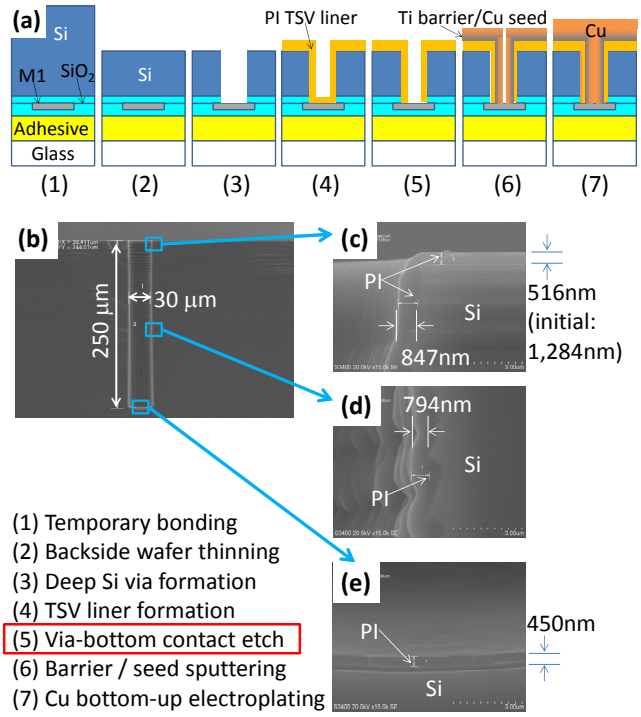

Fig. 5 A process flow of the via-last/backside-via TSV formation for Si interposers (a), and cross-sectional SEM images of a deep Si via with a PI liner after via-bottom contact etch for 35 sec: whole via (b), via top (c), via middle (d), and via bottom (e).

References

[1] T. Matsumoto *et al.*, "Three-Dimensional Integration Technology Based on Wafer Bonding Technique Using Micro-Bumps", *SSDM 1995*, pp.1073-1074.

[2] K.-W. Lee *et al.*, "Impacts of 3-D Integration Processes on Memory Retention Characteristics in Thinned DRAM Chip for High-Reliable 3-D DRAM", *IEEE Trans. Electron Devices*, **Vol.61** (2014), pp.379-385.

[3] T. Fukushima *et al.*, "Reconfigured-Wafer-to-Wafer 3D Integration Using Parallel Self-Assembly of Chips with Cu-SnAg microbumps and a NCF", *IEEE Trans. Electron Devices*, **Vol.61** (2014), pp.533-539.

[4] M. Mariappan *et al.*, "Deteriorated Device Characteristics in 3D-LSI Caused by Distorted Silicon Lattice", *IEEE Trans. Electron Devices*, **Vol.61** (2014), pp.540-547.

[5] T. Fukushima *et al.*, "Low-Temperature and High-Step-Coverage Polyimide TSV Liner Formation by Vapor Deposition Polymerization", *SSDM 2013*, p.866-867.