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Investigation of the Plasma Damage by Etching Process for TSV Formation in Via-last Backside-via 3D IC

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Abstract

We have investigated the effect of plasma damage in TSV formation on MOSFET characteristics to discuss the new antenna rule for the 3D IC design. An IC chip for evaluation was bonded to Si interposer with Cu/Sn microbumps at 280°C for 190 sec and thinned to 50-μm thickness. Via holes through a Si substrate for TSV are formed by ICP-RIE at the backside surface of the IC chip. Diameter and number of via holes are 25 μm and 1, 6, 11, and 21, respectively. These via holes interconnected the first metal which interconnect the gate metal of MOSFET fabricated on IC chip. We measured the I_d-V_g characteristics of the MOSFET before and after via-holes formation. The measurement results show no significant change even after via-holes formation. It is indicated that the via-hole-etching process doesn't affect MOSFET characteristics, because the gate capacitance of MOSFET is much smaller than parasitic capacitance of the first metal.

1. Introduction

Three-dimensional IC (3D IC) has attracted much attention as novel system integration technology since it can realize advanced IC without further scaling down of transistor size. 3D IC consist of vertically stacked thin chips in which through Si via (TSV) vertically interconnect the stacked chips. 3D IC has many advantages such as short wiring length, small chip size, and small pin capacitances. These structural advantages of 3D IC bring both low power consumption and high processing speed even for the IC with highly scaled transistor and interconnections [1]-[3]. However, the reliability of 3D IC has not been evaluated enough yet to penetrate the market.

An increase of the number of TSVs in one interconnection can boost the yield of TSV contact to the metal line. However, an antenna rule for TSV formation has not been established, because the influence of the plasma damage in the TSV formation has not been clarified. In the case of backside via process, charge up by plasma increase with increase of the number of TSVs. So, we should evaluate the effect of charge up by plasma on transistor characteristics to boost the yield ratio of TSV formation. In this study, we have investigated the influence of plasma damage by etching process to form the TSV by measuring *I-V* characteristics before and after etching process.

2. Experimental

In this study, we fabricate the test structure to evaluate the effect of plasma damage as shown in Fig.1. The structure is composed of an IC chip for evaluation, Cu/Sn microbumps and Si interposer. An IC chip was flip chip bonded to Si interposer at 280°C for 190 sec and thinned to 50-μm thickness by mechanical grinding and chemical mechanical polishing (CMP) which coil and bias power-source frequency is 13.56 MHz and 380 kHz, respectively. Via hole through Si substrate interconnect the first metal which directly interconnect the gate electrode of the MOSFET in the IC chip. This via hole is etched by bosch process using inductive coupled plasma reactive ion etching (ICP-RIE). The test structure layouts were shown in Fig.2. Via hole diameter is 25 μm. Lateral and longitudinal pitch of via holes is 75 μm and 50 μm, respectively. The number of via holes are 1, 6, 11, or 21. The area of first metal which interconnect the gate electrode increase with increase of the number of via holes as shown in Fig.2. Finally, we measured relationship between drain current and gate voltage (I_d-V_g) characteristics of MOSFET in the IC chip before and after via hole etching.

3. Result and discussion

Figure 3 shows the birds-eye view of the test structure, and Fig.4 shows the bottom and cross sectional SEM image of the test structure. We could observe that via hole interconnect first metal of IC chip. Figure 5 shows I_d-V_g characteristics of the nMOSFET with L_g/W_g of 0.1 μm/0.9 μm before and after the 21 via holes formation. We could observe no significant change of drive current, threshold voltage (V_{th}) and sub threshold slope characteristics. This result demonstrate that via hole etching doesn't affect MOSFET characteristics in this case. Figure 6(a) and (b) show the relationships between the number of via hole and the change ratio before and after via hole etching process of threshold voltage and drive current of MOSFET in the test structure. Each change ratio of threshold voltage and drive current is less than 5%, and each change ratio didn't change with increase in the number of via holes.

On the basis of these results, it is inferred that most electrical charge affect the parasitic capacitance around first metal in IC chip more than the gate capacitance. Therefore, the capacitance ratio between the capacitance around first metal and gate capacitance is important, and when the capacitance around first metal is sufficiently large, the

plasma damage becomes negligible.

4. Conclusions

In this study, the influence of via hole etching process on MOSFET characteristics was evaluated to realize the high reliability 3D IC. As a result, via-hole etching process didn't affect the MOSFET performance as the capacitance around first metal was usually larger than gate capacitance in conventional IC. Therefore, it was indicated that increase of the number of TSV did not degrade the MOSFET characteristics and would enhance the yield of TSV contact to the first metal in via-last backside-via 3D IC process. This result becomes one of the design guidelines for 3D IC.

References

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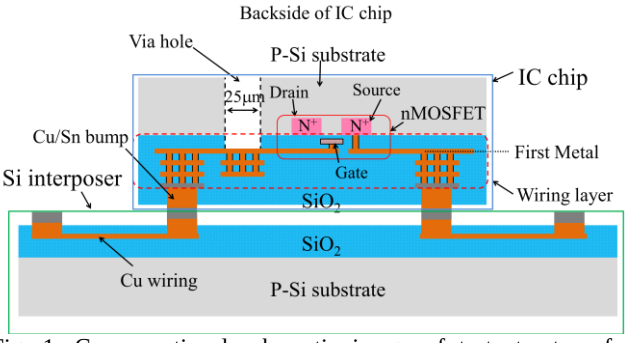

Fig. 1. Cross sectional schematic image of test structure for plasma damage evaluation in TSV formation.

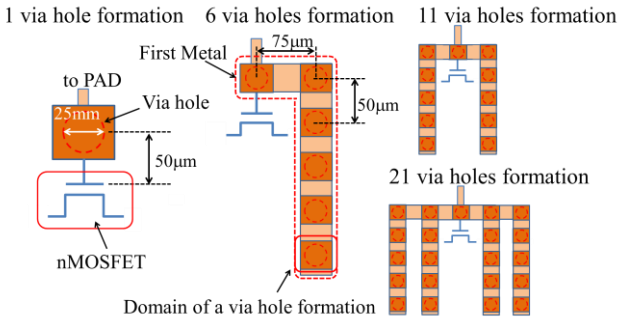

Fig. 2. Via hole and first metal layouts of the test structure.

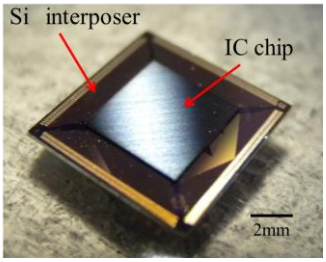

Fig. 3. Photograph of the IC chip bonded on Si interposer.

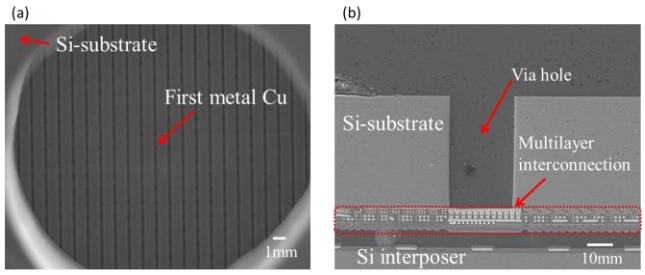

Fig. 4. SEM images of (a) bottom of via hole and (b) cross-section of the test structure.

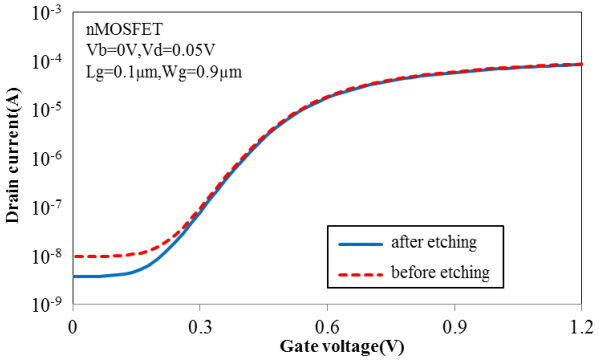

Fig. 5. Id-Vg characteristics of MOSFET before and after 21 via-holes etching.

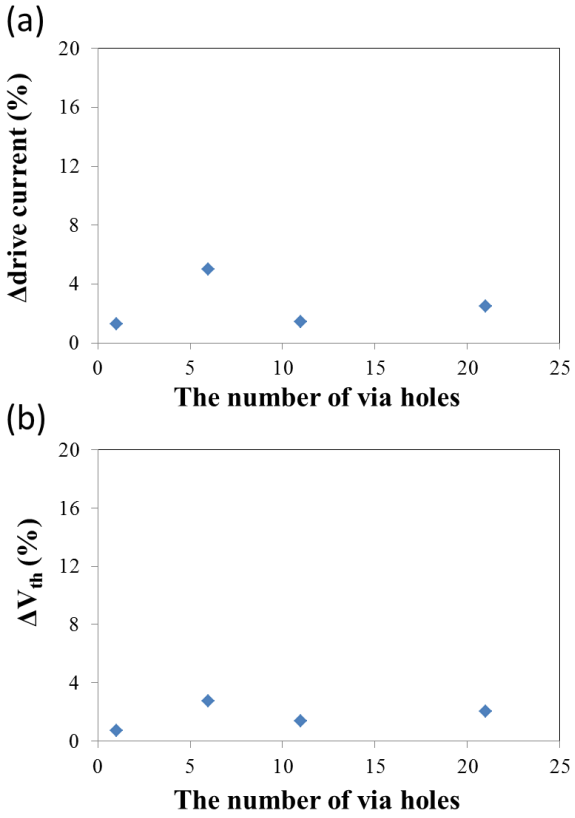

Fig. 6. Effect of the number of via holes on change ratio of (a) drive current, and (b) threshold voltage before and after via-hole etching.