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Suppression of Cu Ion Drift by Metal-Cap on Cu lines, Improving Interconnect Dielectric Reliability

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Abstract

TDDB degradation mechanism was studied with CoWB-metal capped Low-k/Cu interconnects. The leakage current between Cu interconnects without the metal cap initially climbed up, and then the dielectric breakdowns (TDDB) occurred in low-k dielectrics; a bi-modal failure mechanism. The initial leakage climbing was prevented completely by the metal-cap, and TDDB occurred directly; a single-mode failure mechanism. The metal cap blocks Cu-ion drift pass from the Cu surface, and TDDB life-time is determined by intrinsic dielectric properties of the low-k material. We have applied the metal-capped Cu interconnects with super EM reliability to a 40nm-node commercial LSI, confirming no yield degradation.

1. Introduction

The demand for high reliability of Cu/low-k interconnects is growing in automotive MCUs used in high temperature environment and high current driver ICs. Metal-cap processes, in which the Cu surface is covered with thin Co-based films such as CoWB and CoWP, are recognized as a reliability booster against electro-migration (EM) of Cu interconnects [1]. The metal cap process, on the other hand, tends to degrade its dielectric reliability because of the metal contamination on/in the dielectrics during the metal cap process, which can be suppressed by a process refinement. In addition, recently, we find a positive side of the metal cap on dielectric reliabilities; the metal cap can suppress Cu ion drifts during thermal and electric stress. In this paper, we discuss the effects of the metal cap on time dependent dielectric breakdown (TDDB) reliability.

2. Experimental

Cu interconnects with low-k SiOCH films (k~3.0) were fabricated. After chemical mechanical polishing (CMP) to remove Cu, Ta barrier metal, and SiO_2 hard mask on the low-k film, CoWB thin film of about 5 nm thick was deposited directly on the Cu surface by a wet chemical process. After the CoWB cap deposition, SiCN dielectric cap was deposited to cover the entire surface of the interconnect structure as shown in Fig. 1.

TDDB tests were performed in a comb-wiring pattern with 132 nm pitch lines and 90 mm total length. Leakage currents with or without the metal cap were monitored during the TDDB. Here, the TDDB life-time was determined at the time when the leakage current was over 1e-5A.

3. Results and Discussion

Fig.2 shows examples of leakage current vs. duration time under the stress of 3.27 or 0.6 MV/cm at 200^{o}C for (a) the samples (a) without CoWB, and (b) with CoWB. As shown in Fig.2 (a), the leakage current change of the conventional Cu interconnects is characterized by a gradual current increase before a sudden dielectric breakdown. In contrast, the CoWB capped Cu interconnects don't show this gradual current increase before abrupt current jump as shown in Fig. 2 (b). Fig. 3 shows the time to failure distributions in TDDB test under 200^{o}C, 3.27MV/cm stress. Fig. 4 shows TDDB characteristics of Cu interconnects with CoWB and without CoWB. Fig. 4 (a) shows $T_{63.2}$ as a function of square-root of electric field, and Fig. 4 (b) shows $T_{63.2}$ as a function of 1000/T, respectively. The CoWB capped Cu interconnects show comparable TDDB lifetime as those without CoWB under this TDDB definition.

(a) A Mechanism of Cu drift suppression with CoWB

Fig. 5 illustrates a model for the suppression of Cu ion drifts in CoWB capped Cu interconnects. The previous studies correlate this gradual current increase with Cu ion drifts phenomena [2] [3], in which Cu ions migrate under a field stress and recombine with electrons to form Cu particles. Accumulated Cu particles create a metallic shorting bridge or cause effective dielectric thinning. Another study suggests Cu ions piled up near cathode electrode modify the conduction band and conduction mechanism changes from Poole-Frenkel emission to Fowler-Nordheim emission which brings a current increase [3]. In the metal-capped Cu interconnects, the Cu surface oxidation is suppressed, and the ionization of Cu atoms hardly occurs, preventing the Cu-ion drift. Thus, the TDDB life-time is determined simply by intrinsic dielectric properties of the low-k material. This single-mode failure simplifies the life-time estimation for Cu interconnects with no consideration of the complicated Cu-ion drift issue.

(b) Evaluation in A 40 nm-node LSI

CoWB caps were adopted in M1 to M5 of the test wafer of a 40 nm-node high-speed network processor as shown in Fig. 6. Fig. 7 shows yield of wafer-level function tests related to open, short failures. The test wafer with CoWB cap shows comparable yield as the product wafer.

4. Conclusions

CoWB cap suppresses Cu ion drifts during bias temperature stress with no deterioration of TDDB characteristics, TDDB of Cu interconnects is not determined by Cu ion drifts. The Cu-ion-drift-free, metal-capped interconnects with super EM reliability demonstrate no yield degradation in a 40nm-node commercial LSI.

Acknowledgements

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References

[1] M. Ueki, *et al.*,IITC2011, pp.55-57.
[2] F. Chen, *et al.*, IRPS2005, pp.501-507.
[3] N.Suzumura, *et al.*, IRPS2006, pp.484-489.

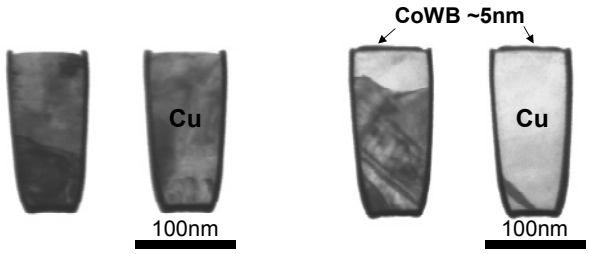

Fig. 1 Cross-sectional TEM images of test structures. 132nm pitch Cu/non-porous SiOCH (k~3.0) damascene interconnects (a) without CoWB, and (b) with CoWB are evaluated.

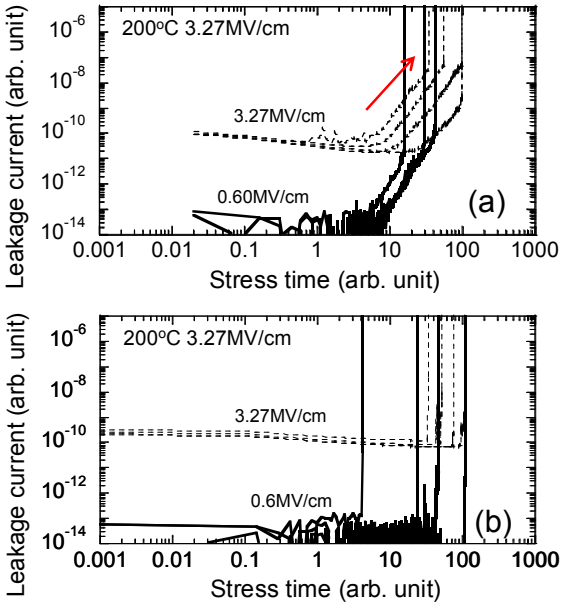

Fig. 2 Examples of leakage current vs. duration time under the stress of 200°C, 3.3MV/cm for (a) the samples without CoWB, and (b) those with ~5nm CoWB.

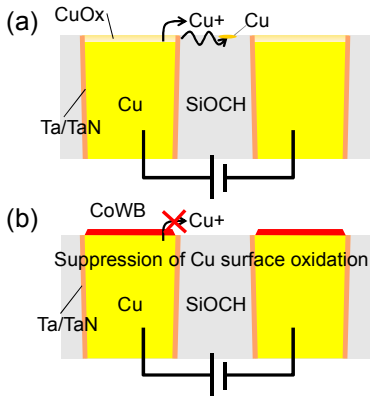

Fig. 5 A model for the suppression of Cu ion drifts in CoWB capped Cu interconnects. (a) Conventional Cu interconnects without CoWB, (b) CoWB capped Cu interconnects. Cu surface oxidation is suppressed by the CoWB.

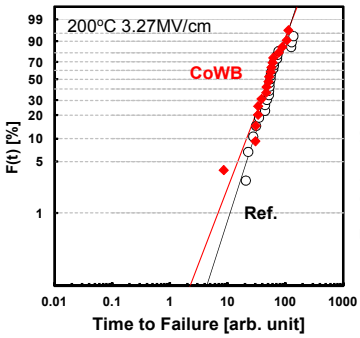

Fig. 3 Time to failure distributions in TDDB test at 200°C, 3.27MV/cm stress..

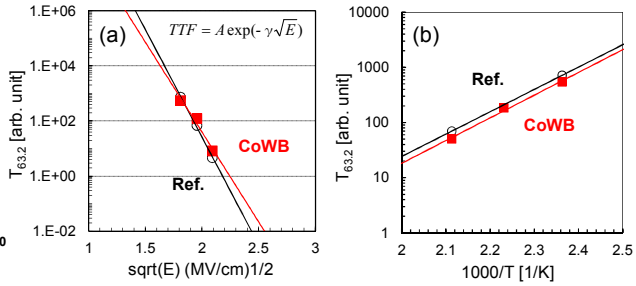

Fig. 4 TDDB characteristics. (a) $T_{63.2}$ as a function of square-root of electric field. (b) $T_{63.2}$ as a function of 1000/T.

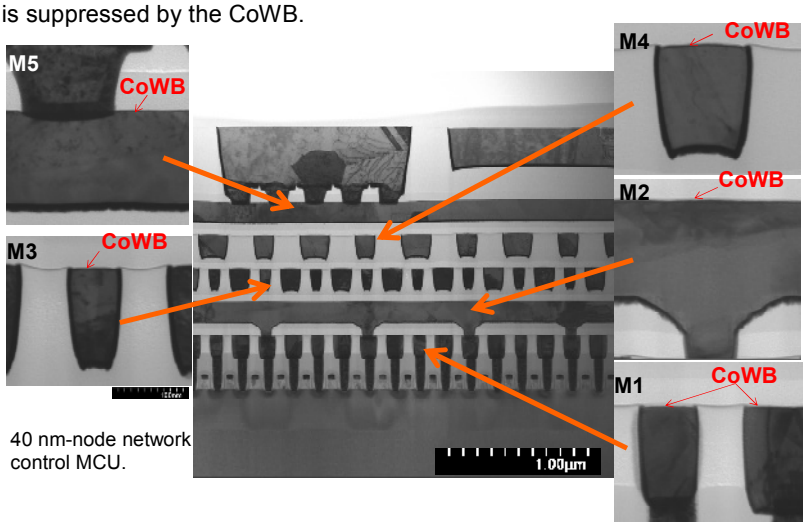

Fig. 6 Cross-sectional TEM images of the test wafer of 40 nm-node high-speed network control processor. CoWBs were applied to M1 through M5.

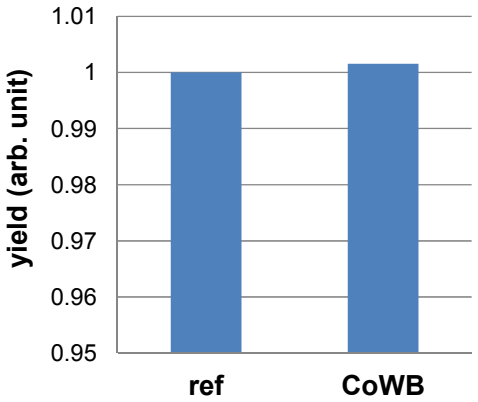

Fig. 7 Chip yield of function tests related to open, short failures of the test wafer of 40 nm-node network processor. The CoWB cap split show comparable yield as the product wafer.