Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp772-773

Fabrication and Characterization of MoS_2 FET structure with Nano-Sheets $Ca_2Nb_3O_{10}$ Gate Insulator

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Abstract

Dielectric nano-sheets $Ca_2Nb_3O_{10}$ (ns-CNO) was supported on several layers MoS_2 transferred on SiO_2/p-Si substrate by dip-coating at room temperature. We have demonstrated the fabrication of MoS_2 FET structure with ns-CNO gate insulator. The ns-CNO worked as a gate-insulator with good insulating property. Fabricated MoS_2 FET structure indicated n-type FET behavior, and exhibited a current on/off ratio of approximately 1000 by applying the gate voltage of ±4.5 V.

1. Introduction

Two-dimensional layered semiconducting materials such as graphene, BN, and MoS_2, have been extensively studied since thickness of these materials can be readily decreased to atomic length order, which is suitable to realize the nano-scale MOSFET device formation. Especially, single-layer MoS_2 works as a direct gap semiconductor with bandgap of 1.8 eV,[1] and Kis *et al.*, reported the fabrication and characterization of single-layered MoS_2 FET structure.[2] However, for formation of ultra-thin semiconductor FET, the main problem is difficulty of deposition of gate insulator on the layered semiconducting materials due to their extreme vulnerability. In the device formation process, it causes the defects in the semiconductor/insulator interface, readily. In order to solve this problem, we propose the formation of gate insulator on the MoS_2 using dielectric nano-sheet $Ca_2Nb_3O_{10}$ (ns-CNO) by soft-chemical process. The ns-CNO has a ultra-thin two-dimensional structure with a lateral size of several μm scale, and it can be supported on the various substrate materials by dip coating using an aqueous ns-CNO dispersion solution at room temperature.[3-6] In this study, we report the fabrication and characterization of MoS_2 FET with ns-CNO gate insulator structure on the SiO_2/Si substrate.

2. Experimental

Firstly, p-Si substrates were dipped in a diluted HF solution for removing the native oxide layer. After the HF dipping, thermal oxide layer with thickness of 240 nm was prepared by thermal annealing at 1100 ºC for 210 min in O_2 gas flow.

In this study, a natural bulk crystal of MoS_2 was used,

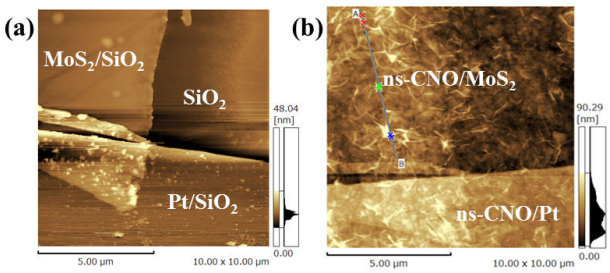

Figure 1 AFM images for (a) MoS_2 on the SiO_2/p-Si substrate, and (b) ns-CNO on the MoS_2.

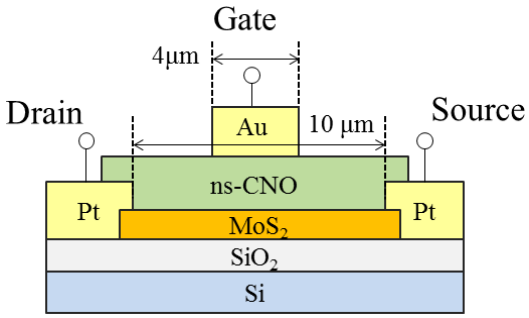

Figure 2 Schematic illustration of MoS_2 FET with ns-CNO gate insulator.

and it was transferred to the SiO_2/p-Si substrate by conventional tape-casting method. After the several times of tape-casting treatment, in the atomic force microscopy (AFM) observation, MoS_2 with 12.7 nm (equal to 20 layers) were obtained on the substrate as shown in Fig. 1 (a). Pt source and drain electrodes were prepared on the MoS_2 by conventional pulsed laser deposition method and photolithography technique.

After the formation of source and drain electrode, ns-CNO layers were supported on the specimen by dip-coating using an aqueous ns-CNO dispersion solution.[3,4] Figure 1 (b) shows the AFM image of ns-CNO supported on the MoS_2. Observed result indicates all of surface was covered with ns-CNO flakes with 1-2 μm size. Also, thickness of ns-CNO was 11.7 nm (equal to 8 layers) from *z*-axis height profile analysis. Finally, Au gate electrode with 4 μm width was deposited on the ns-CNO gate insulator by conventional thermal evaporation. A schematic depiction of the fabricated FET device structure is shown in

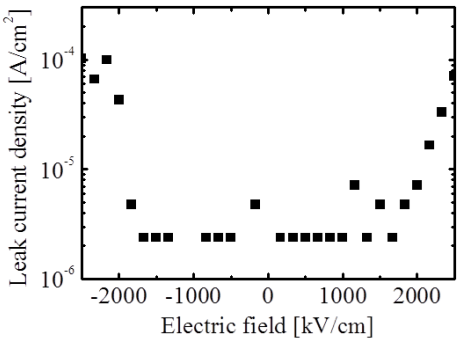

Figure 3 *J-E* property of Au/ns-CNO/MoS_2 hetero-layered structure.

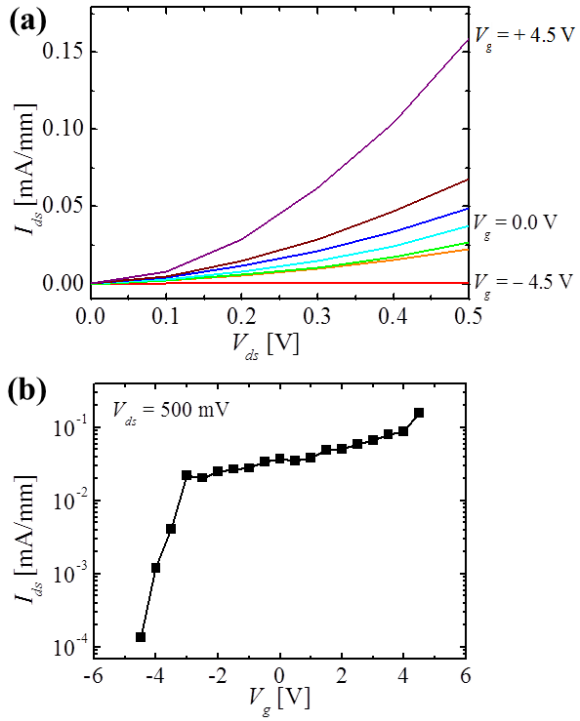

Figure 4 (a) I_{ds}-V_{ds} curves and (b) I_{ds}-V_g curve of MoS_2 FET with ns-CNO gate insulator.

Fig. 2.

We performed electrical measurement of specimen by using pA-meter (Agilent HP4140B) with gate voltage source at room temperature.

3. Results and Discussion

Figure 3 shows the leakage current density versus electric field (*J-E*) curve of Au/ns-CNO/MoS_2 gate structure. In the range of applied electric field less than 2000 kV/cm, the ns-CNO indicates excellent insulating property without any conducting pass in the boundary even though ns-CNO was a flake-like and ultra-thin layered structure.

Figure 4 (a) is drain current versus drain voltage (I_{ds}-V_{ds}) curves of MoS_2 FET with ns-CNO gate structure with changing the applied gate voltage V_g in the range from -4.5 V to +4.5 V. As shown in the figure, the specimen shows a typical behavior of FET with n-type channels. These results indicate the new type of FET structure using nano-sheet materials can be prepared by present soft-chemical method.

Figure 4 (b) shows I_{ds}-V_g curve of specimen. Here, measurement was carried out at the fixed V_{ds} of 0.5 V. A current on/off behavior was clearly observed, and highest on/off current ratio was approximately 1000 by applying the gate voltage in the range from –4.5 V to +4.5 V. Observed on/off current ratio is higher than that of ALD-Al_2O_3 top gate MoS_2 FET structure (about several hundred).[7] This means that the present ns-CNO soft-chemical supporting process can reduce the degradation of insulator/MoS_2 interface compared to conventional film deposition process.

3. Conclusions

We have demonstrated the fabrication of MoS_2 FET with ns-CNO gate insulator structure on the SiO_2/Si substrate. The ns-CNO worked as a gate-insulator with good insulating property. Fabricated MoS_2 FET structure indicates n-type FET behavior, and exhibits a current on/off ratio of approximately 1000 by applying the gate voltage of ±4.5 V.

Acknowledgements

This work was partly supported by a research grant from the Hokuriku bank young scientist foundation. The authors would like to thank Professor H. Okudera of Kanazawa University for his considerable help and technical assistance.

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