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Tunnel-FET Transistors for 13nm Gate-Length and Beyond

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Abstract

Reducing supply voltage (V_{dd}) while keeping leakage current low is critical for minimizing energy consumption and improving battery life in mobile devices. A Tunnel-FET (TFET) is not limited by the thermal tail and can perform better than a MOSFET at low V_{dd}. In this paper, we use atomistic quantum models to compare logic circuit energy-delay with TFET and MOSFET for Lg=13nm. Scaling down to Lg=9nm (ITRS year 2022) is discussed and Resonant-TFET idea that enables steeper sub-threshold slope (SS) at ultra-scaled dimensions is introduced.

1. Introduction

Although numerous experimental TFETs have been demonstrated SS<60 mV/dec, it has been challenging to achieve both steep-SS and high drive current together due to the requirement of novel materials with thin body geometry and low-defect channel materials. Here, we compare one large scale experimental III-V TFET to atomistic quantum simulations to validate agreement without the addition of any defects. Then atomistic models are used to compare TFET and MOSFET for future nodes including logic circuit energy-delay and scaling.

2. Atomistic Models and comparison to Experiments

A detailed comparison between InGaAs TFET's experimental characteristics and atomistic quantum mechanical predictions is reported to understand the validity of using atomistic models to predict performance of a scaled TFET [1]. Simulations did not employ any fitting parameters to match the experimental data, but instead used material and geometry parameters as the only inputs. The results show that the experimental and simulation characteristics are in reasonable agreement, suggesting that the experimental devices are without significant unknown effects or defects, and the atomistic simulations have good predictability (Fig.1).

3. TFET vs. CMOS at Lg=13nm

According to the ITRS roadmap [2], 2018 Low Operating Power targets require Lg=13nm. Different N-TFET material options and Si MOSFET are compared using atomistic quantum models at this node (Fig.2) [3]. Heterojunction N-TFET using a GaSb source and InAs channel and drain has the highest drive current (I_{Dsat}), in line with experimental results.

2. Effect of Device Variations

Effects of device variations on I-V characteristics are studied assuming 10% variation for device dimensions and A_{Vt}~1 for work-function variation (WFV) [3]. For both MOSFET and TFET, WFV is the leading source of variation. TFET is more susceptible to higher leakage current variation when Ioff is targeted close to its steep SS (Fig.3a). MOSFET I_{Dsat} variation is larger at the higher performance targets. Energy-delay circuit simulations show at lower performance targets, even when variations are included, TFET logic shows better energy-efficiency than CMOS.

4. TFET Scaling Down to Lg=9nm and Resonant-TFET

Scaling of Lg for two generations, to 11 and 9nm i.e. ITRS year 2020 and 2022, was investigated. The sensitivity of Het-j TFET characteristics to gate oxide thickness is not significant, thus oxide scaling cannot be used as a knob to enable TFET gate-length scaling. The main knob to recover degraded TFET characteristics due to scaled-Lg is to reduce body-thickness (Fig. 4a) [4]. Compared to DG TFET, NW TFET relaxes the critical body thickness from 1.9nm to 3nm, and improves the device characteristics (Fig.4b).

Fig.5 shows the cross-section and band-alignment for the conventional Het-j TFET and a new device, the Resonant-TFET [4]. R-TFET uses the same material combination as a Het-j TFET, but in reverse order. This band order creates a narrow triangular potential well at the source side of heterojunction, with discrete resonant energy levels. The resonant energy levels are designed to align with the source valance band only when the device is on to enable a faster change in tunneling rate between on and off regions (Fig.6) [4]. At Lg=9nm, the R-TFET achieves an average SS~25 mV/dec, with 100x Idsat advantage over a MOSFET at Vdd=0.27V, extending the scaling path of tunneling transistors beyond the Lg=9nm node (Fig.7).

5. Conclusions

Benchmarking of InGaAs TFET quantum simulations show they are in-line with experiments without any fitting parameters. Using these models, circuit simulations illustrate TFETs are more energy efficient than CMOS at ITRS node for 2018, even when device variation is considered. TFET characteristics are shown to be superior to MOSFET characteristics at very low supply-voltages with scalability through at least 2022 ITRS generation. Thus, TFET is a promising transistor for ultra-low power technologies of the future, but significant experimental effort will be required to achieve target devices using novel materials with thin

body geometry and low-defect density.

References

[1] U. Avci et al, 2012 VLSI Tech. Symp., pp. 183-184.

[2] ITRS roadmap, http://www.itrs.net/reports.html

[3] U. Avci et al, 2013 IEDM, pp. 33.4.1-33.4.4

[4] U. Avci et al, 2013 IEDM, pp. 4.3.1-4.3.4

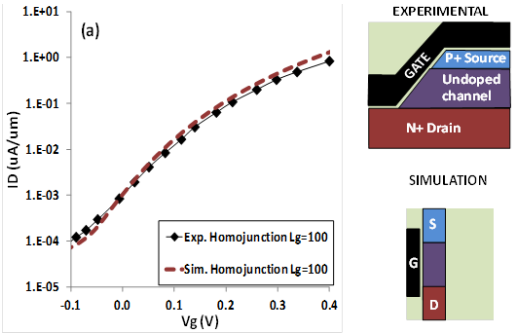

Fig.1 (a) Id-Vg characteristics of the quantum simulation of an InGaAs TFET and an experimental TFET are in reasonable agreement. (b) Both devices have L_{eff}=100nm and EOT=1.4nm.

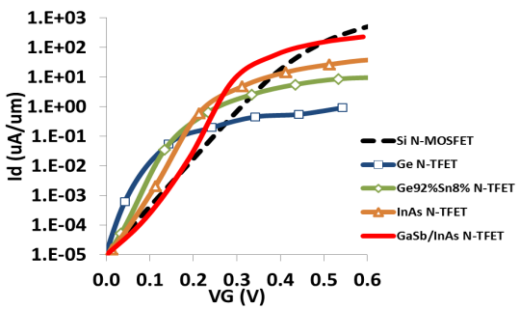

Fig.2 Comparison of drain current for different N-TFET materials and Si MOSFET using atomistic simulations. (V_{ds}=0.3V, Lg=13nm and I_{off}=10pA/um target)

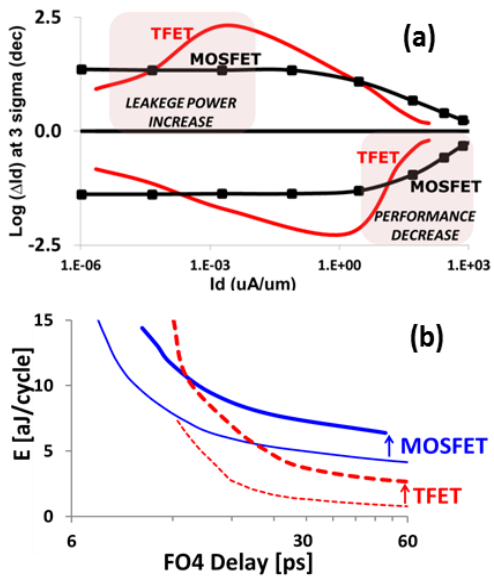

Fig.3 (a) Comparison of 3-sigma WFV effect on MOSFET and TFET drain current. For I_{dsat}>~10uA/um performance targets, MOSFET drive current variation is larger than TFET. (b) Power-performance without (thin lines) and with (thick lines) device variations is shown for 10% logic activity.

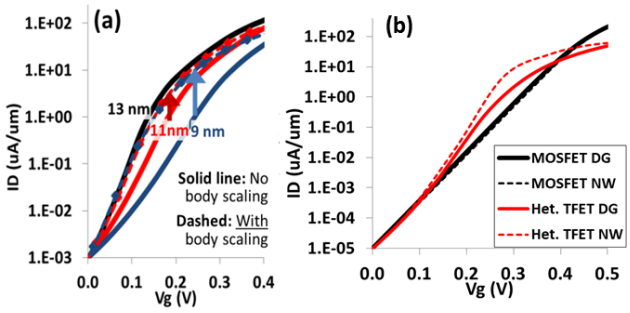

Fig. 4 I-V characteristics (a) for Lg=13, 11 and 9nm DG TFET with scaled gate oxide and body thickness and (b) Lg=9nm TFET and MOSFET each with DG and NW geometries. NW geometry improves TFET characteristics, whereas MOSFET is unchanged.

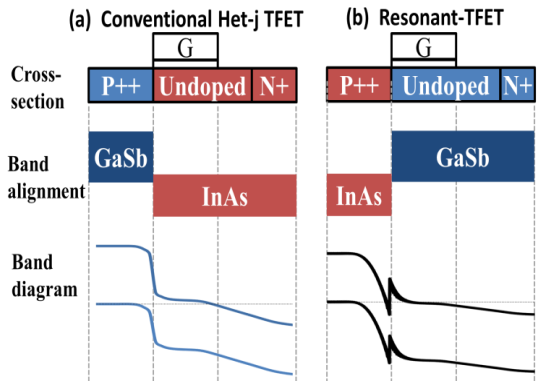

Fig.5 Device cross-section, band-alignments and band diagrams for (a) conventional Het-j TFET and (b) Resonant-TFET. Resonant-TFET uses the same materials but with reverse order.

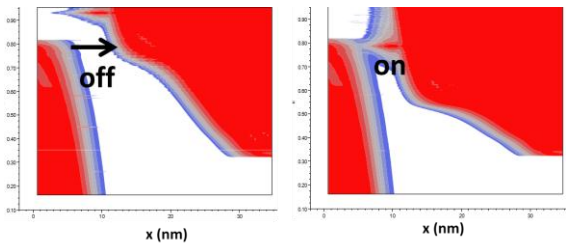

Fig.6 Density of states spectrum along a Resonant-TFET for Lg=9nm NW. R-TFET resonant energy levels are aligned to source valance band, achieving superior I-V characteristics.

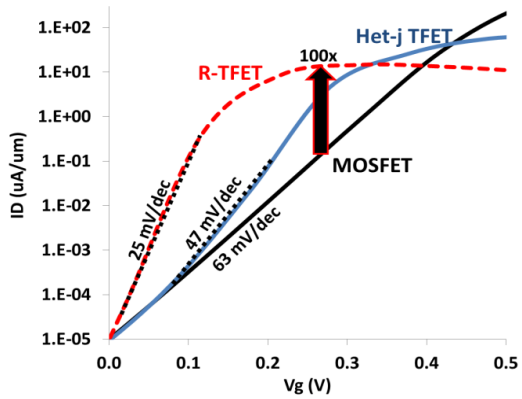

Fig.7 I-V curves for Lg=9nm NW R-TFET, Het-j TFET and MOSFET. R-TFET has 100x higher I_{dsat} than MOSFET at V_{DD}=0.27V. (I_{off}=10pA/um, V_{ds}=0.3V)