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Novel Device Architecture Proposal of Source Junctionless Tunneling Field-Effect Transistor (SJL-TFET)

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Abstract

In this paper, we propose novel device architecture of Source Junctionless Tunneling FET (SJL-TFET) featuring notable advantage of electrostatics such as steep sub-threshold swing (*S.S.*), suppressed variability in device characteristics and the availability in LSI production. Theoretical TCAD simulation analysis reveals the mechanism of essential operation and its advantage in device characteristics. Also, significantly suppressed threshold voltage (V_{th}) variation was experimentally demonstrated in SJL-TFET owing to its extremely simple device structure. SJL-TFET enables practical application of all-Si standard fabrication process.

Introduction

Tunneling field-effect transistors (TFETs) have attracted much attention for ultra-low power LSI applications thanks to its possibility of overcoming the limitation of *S.S.* in MOSFET [1]. So far, many types of TFET device architecture have been reported utilizing a variety of structures and new material introduction [2-7]. However, there has been an essential trade-off between *S.S.* improvement and process complexity, i.e. these types of device and process techniques tend to cause an undesirable fluctuation in device characteristics. Consequently, from the viewpoint of LSI production, these types of TFETs would not be available for low voltage circuit operation due to serious V_{th} variability even if super-steep *S.S.* could be achieved [8].

In this paper, a novel TFET device concept is proposed featuring both steep *S.S.* and suppressed device variation. This simple device structure without forming source tunneling junction enables the practical LSI application of TFET.

Energy Minimum Optimization in TFET

In order to estimate the impact of V_{th} fluctuation on power-performance figure of merit, theoretic analytical TFETs model was introduced. Original idea in MOSFET by Fuketa et al. [8] expands into TFET case with modification of on/off-current expression shown in Fig. 1(a). For ideal TFET, on-current is dominated by band to band tunneling (BTBT) current, so that current-voltage expression is well-fitted with Kane's approximation $I \sim V^P \exp(-B/V)$ [9] utilizing some fitting parameters (**Fig. 1(b)**). Since TFET has good immunity against DIBL (Drain Induced Barrier Lowering), the off-current simply consists of BTBT current. Therefore, off-current could be sensitive for its sub-threshold factor (S_{off}) at $V_g = 0$ V (see **Fig. 1(a, b)**). Switching energy (power-delay product) is calculated for logic application using expression stated above (activation rate = 0.2). **Figure 1 (c)** shows the energy-voltage relationship with various V_{th}–fluctuation tolerance (δV_t). From this result, significant sensitivity of V_{th} on energy (PD product) and V_{DD} minimum are expected. Also, energy minimum analysis was quantitatively carried out at various *S.S.* (S_{off}) by using this method (**Fig. 2**). If 15% degradation of minimum V_{DD} (V_{opt}) caused by V_{th} fluctuation is accepted (solid red line in figure 2), worst corner of δV_t corresponding to 3σ (V_{th}) fluctuation is -26 mV, -21 mV, -15 mV and -10 mV for the device with 60 mV/dec., 50 mV/dec., 40 mV/dec. and 30 mV/dec., respectively. This result clearly indicates that steeper-*S.S.* device requires reduced V_{th} fluctuation rather than relatively broader *S.S.* device.

Device Concept of Source Junctionless (SJL) TFET

Schematic device structure of SJL-TFET is illustrated in **Fig. 3-(ii)** with diffusion shape contour plot. This device essentially has uniformly doped source region for entire device active area. Drain diffusion region is simply located beside gate electrode like a conventional Lateral TFET (PiN-TFET) structure (**Fig. 3-(i)**). At the off state in SJL-TFET (**Fig. 4-(a)**), channel region just under the gate electrode stays depleted condition. Here, negligible tunneling current from source to drain is observed. With increased gate voltage (**Fig. 4-(b)**), the inversion layer appears entire channel region. In this situation, tunneling path is created from source to inverted channel region which is parallel to the electric field caused by applied gate voltage (**Fig. 4-(c)**). BTBT generation rate in source region is plotted in **Fig. 4-(d)**. Uniform BTBT generation is confirmed entire channel region. In terms of *S.S.* improvement, this architecture can eliminate the long range tunneling path which degrades *S.S.* usually observed in conventional PiN-TFET [10]. Simulated I_d-V_g characteristics of proposed (SJL-TFET) and conventional (PiN-TFET) devices are shown in **figure 5**. Here, non-local Kane tunneling model [9, 11] is combined with the drift-diffusion model. Both *S.S.* reduction and I_{on}-I_{off} ratio improvement are clearly observed in SJL-TFET.

In order to evaluate the circuit guard band tolerance, worst corner analysis on process variation sensitivity was investigated in various conditions of source junction formation and EOTs (**Fig. 6**). Here, SJL-TFET exhibits significantly suppressed V_{th} and *S.S.* variation in spite of steeper *S.S.* range. In addition, EOT scaling in SJL-TFET effectively minimizes *S.S.* value and suppresses both *S.S.* and V_{th} variation.

Experimental Demonstration Results

To demonstrate the theoretical advantage of SJL-TFET, hardware experiment was carried out using standard Si-CMOS technology platform (**Fig. 7**). In this experiment, SOI wafer of T_{Si} / T_{BOX} = 80 nm/145 nm was used for starting material. At the first step, uniformly doped source region was formed with conventional ion implantation and annealing techniques for entire active area. Next, drain deep diffusion region was formed with lithography and implantation process. Then, gate stack of HfO_2/TiN was employed with 1.3 nm EOT. As a reference, PiN-TFET was also fabricated by adding lithography for source formation. Note that, the concentration of source diffusion region is ~1e19 cm^{-3} for SJL-TFET and ~1e20 cm^{-3} for PiN-TFET, which is quite different in order to optimize for each structure. Also, scaled EOT of 1.1 nm was adapted to PiN-TFET.

Experimental I_d-V_g curves of fabricated N-channel SJL-TFET and PiN-TFET are shown in **figure 8**. In SJL-TFET, I_{off} of ~0.01 pA/μm was successfully achieved which is more than 3-orders smaller value than standard low standby power (LSTP) CMOS lineup. Minimum of *S.S.* value of 140 mV/dec. was achieved in SJL-TFET, while PiN-TFET showed 220 mV/dec. I_d-V_d curves at various V_g shows good linearity and saturation property like MOSFET (**Fig. 9**). In general, all-Si N-channel TFETs suffers from relatively large *S.S.* value than P-channel TFETs. This is mainly explained by the difficulty of steep tunnel junction formation in source regions by boron. SJL-TFET has significant advantage of archiving smaller *S.S.* because of no junction formation architecture.

Electrostatics variability was evaluated focusing on global V_{th} (**Fig.10**) and local V_{th} (**Fig.11**). As discussed in TCAD analysis, tight electrostatic distribution has been confirmed in SJL-TFET. 3σ (V_{th}) of 17.8 mV was obtained in SJL-TFET. This value can be acceptable in the steep *S.S.* devices down to 45mV/dec. if 15% V_{opt} degradation is allowed. (See in **figure 2**). This result is the critical evidence of ultra-low voltage circuit operation availability below 0.3 V range.

Conclusion

Novel device architecture of source junctionless tunneling field-effect transistor (SJL-TFET) has been proposed. Because of its simple device structure, essential advantage of SJL-TFET of steeper *S.S.* and suppressed variability has been confirmed by both theoretical simulation analysis and experimental demonstration.

Acknowledgement

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References [1] L. Wei et al., IEDM (2010) pp. 391., [2] W-Y. Choi et al., IEEE EDL 28 (2007) pp. 743., [3] Q. Huang et al., IEDM (2012) pp. 187., [4] S. H. Kim et al., VLSI Tech., (2009) pp.178., [5] R. Iida et al., SSDM (2011) pp. 843., [6] G. Zhou et al., IEDM (2012) pp. 777., [7] Y. Kondo et al. SSDM (2013)., [8] H. Fuketa et al., IEDM (2011) pp.559., [9] E. O. Kane et al., J. Phys. Chem. Solids 12 (1957) pp.181., [10] C. Hu et al., IEDM (2010) pp.387. [11] A. Biswas et al., Microelectro. Eng. 98 (2012) pp.334., [12] Y. Morita et al., SSDM (2012) pp. 801..

(a)

- TFET *I-V* expression (this work)

$$I_{\rm on} \propto (\alpha V - V_{\rm t1} - \delta V_{\rm t})^P \times \exp\left(-\frac{B}{V - V_{\rm t2} - \delta V_{\rm t}}\right)$$

$$I_{\rm off} = I_0 \times 10^{-\delta V_{\rm t}/S_{\rm off}}$$

- Power-Delay Product [8]

$$E = P \cdot D \propto V_{\rm DD}{}^2(\xi + I_{\rm off}/I_{\rm on})$$

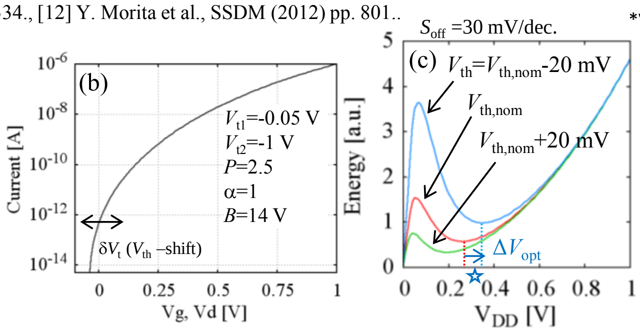

Fig. 1: (a) Simplified *I-V* and energy model for TFET in this study based on [8]. V_{th}-shift (δV_t) is considered in on and off current. Energy is calculated from product of Power ($P \sim \xi I_{on} V_{DD} + I_{off} V_{DD}$; ξ~activation ratio) and Delay ($D \sim V_{DD}/I_{on}$). (b) *I-V* curve of TFET is determined by fitting parameters. The V_{th}-shift of *I-V* curve is defined as δV_t. (c) Power(*P*)-delay(*D*) product for logic application (ξ ~ activation ratio=0.2, S_{off}=30 mV/dec.) for various V_{th}-shift. $V_{th,nom}$ is defined as nominal threshold voltage at $\delta V_t = 0$.

*Vopt is the local minimum point in PD-plot.

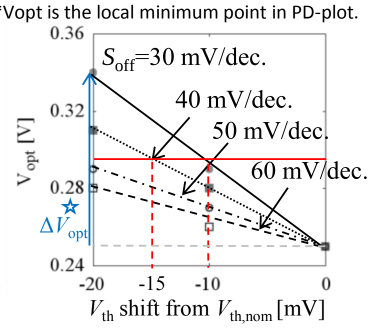

Fig. 2: Threshold voltage shift δV_t dependence of optimum V_{DD} (V_{opt}) in PD product. The shift is sensitive for *S.S.* of off-current (S_{off}). This shows steep-S devices are owed to disadvantage in V_{DD} reduction.

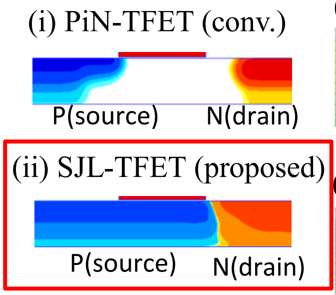

Fig. 3: Schematic structure of N-channel TFET. (a) Conventional PiN-TFET. (b) Proposed source junctionless (SJL) TFET. In SJL-TFET, Source are uniformly formed.

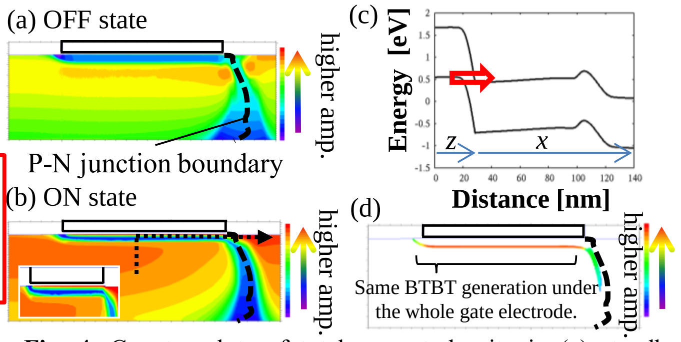

Fig. 4: Counter plots of total current density in (a) standby mode and (b) operation mode. In ON-state, electrons generated from BTBT flow under the gate region (inset of Fig.4(b)). (c) Energy band diagram along to current path shown in Fig.4(b). (d) BTBT generation rate in source region.

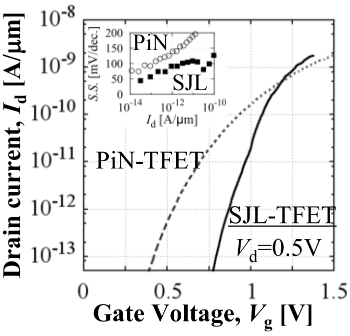

Fig. 5 (Sim.): I_d-V_g characteristics of PiN-TFET and SJL-TFET for L_g=150nm. SJL-TFET achieves steeper sub-threshold swing (inset of figure.).

(a)

	PiN-TFET	SJL-TFET
Source I/I dosage (cm⁻³)	1.8x10¹⁵ 2.0x10¹⁵ 2.2x10¹⁵	0.9x10¹⁴ 1.0x10¹⁴ 1.1x10¹⁴
OSS* thickness (nm)	5 10 15	20 25 30
Activation temp. (°C)	1000 1100	1000 1100
EOT (nm)	1.0 1.4	1.0 1.4

*OSS : Offset spacer for source I/I in PiN-TFET and for drain I/I in SJL-TFET.

*S.S. and V_{th} at I_d=1x10^{-12}(A/um)

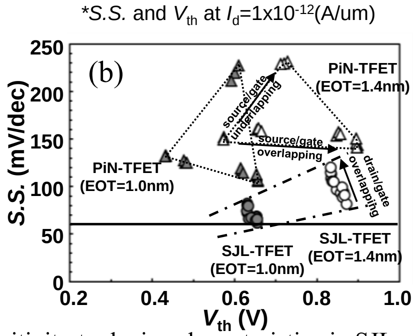

Fig. 6 (Sim.): Process sensitivity to device characteristics in SJL-TFET and PiN-TFET. (a) Simulated worst corner of key parameters in TFETs. (b) Sub-threshold slope (*S.S.*) and V_{th} including process variability. Significantly smaller sensitivity is confirmed in SJL-TFET. Also, EOT scaling achieves even smaller *S.S.* and V_{th} variation in SJL-TFET.

- SOI/BOX (80nm/145nm)
- Ion implantation for source formation
- RTA (1050°C 1min.)
- EB Litho. for drain ion implantation.
- Ion implantation for drain formation
- RTA (1000°C 10sec.)
- Gate stack (TiN/HfO$_2$)
- BEOL (M1)

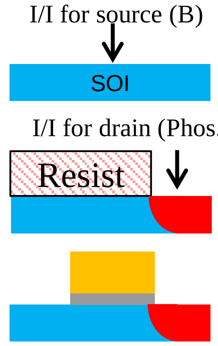

Fig. 7: Process flow of SJL-TFET. S/D and gate area is defined by EB lithography [12].

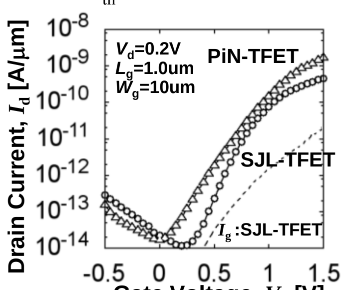

Fig. 8. (Exp.) : I_d-V_g characteristics of PiN-TFET and SJL-TFET.

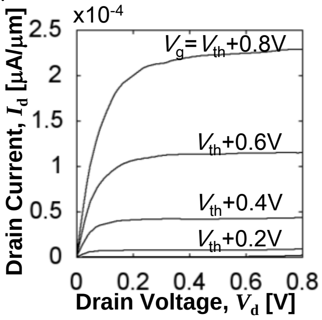

Fig. 9. (Exp.) : I_d-V_d characteristics of SJL-TFET.

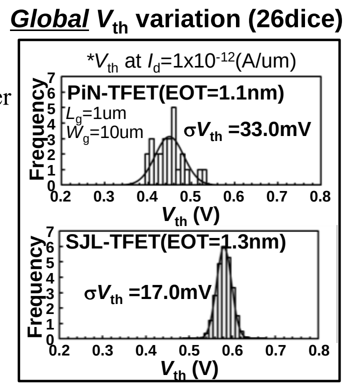

Fig. 10. (Exp.) : Histograms of V_{th} distribution in PiN-TFET and SJL-TFET fabricated with same process conditions.

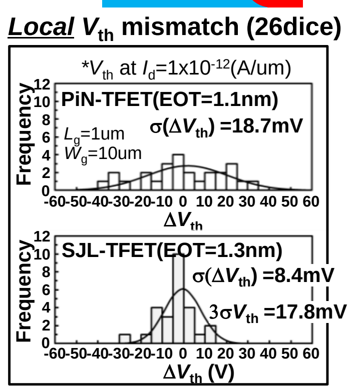

Fig. 11. (Exp.) : Histograms of V_{th} mismatch distribution in PiN-TFET and SJL-TFET. 3σV_{th} of 17.8mV was achieved in SJL-TFET