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Self-aligned Bottom Source Tunnel Field Effect Transistor (Btm-S TFET) with Si:C and Si:P Epitaxial Process

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Abstract

In this paper, we demonstrate self-aligned bottom source tunnel FET (Btm-S TFET). Uniform tunneling current at p-n junctions under gate electrode suppresses V_{TH} variability, which is significant for low power application. Carbon doped Si (Si:C) epitaxial layers were utilized in tunnel junction formation to create steep profile even with the thermal budget in Si-CMOS compatible process.

Introduction

Suppression of off current (I_{OFF}) is indispensable for low power application; and devices operating at minimum I_{OFF} are utilized for specific ultra low power circuit blocks (Fig. 1). Since (a) short channel effect (SCE), (b) gate induced drain leakage (GIDL) currents, (c) gate leakage currents (I_G) are closely related each other, all are needs to be designed. In short channel regions, SCE determines I_{OFF} ((a) in Fig. 1). Higher dosage of channel and Halo doping suppresses SCE, however, gate induced drain leakage (GIDL) increases I_{OFF} ((b) in Fig. 1). In longer channel regions ((c) in Fig. 1), gate leakage currents are dominant. Considering all, relaxed L_G of more than 0.1 μm is commonly used for ultra low power regions (**A** in figure 1). How to achieve lowered I_{OFF} in scaled L_G is important for ultra low power products (**B** in figure 1). TFETs are promising approach to break the dilemma of device design in MOSFET. Controlled SCE and steeper sub-threshold swing (S.S.) [1-3] in TFETs suppresses I_{OFF} increase in scaled L_G; however, the optimization of tunnel junction formation and drain engineering are significant to achieve the advantage of TFETs. In this paper, we propose self-aligned bottom source (Btm-S) TFET for ultra low power application with suppressed variation in device characteristics.

Proposed structure of Btm-S TFET

Good short channel behavior was observed in lateral direction TFET (Fig. 2). However, variability of V_{TH} was confirmed in I_D-V_G curves, and I_{OFF} increases due to varied V_{TH} (Fig. 3). This is explained by disordered tunneling pass at gate edge caused by indented gate edge and dopant profile fluctuation (Fig. 4 (a)). In the proposed structure of Btm-S TFET, areal tunneling current is uniformly generated so that suppression of variability in device characteristics (Fig. 4 (b)) is expected.

Proposed integration scheme of Btm-S TFET

i) *Self-aligned process and drain engineering in Btm-S TFET.*

Source regions are formed close to drain regions in Btm-S TFET; therefore, device design at drain regions is significant [4]. If source regions at drain side are formed at the inside of gate edge (Fig. 5 (a)), unexpected lateral tunneling currents are produced. Consequently, it degrades device characteristics in sub-threshold regions. Whereas, if source regions are extended from the gate edge (Fig. 5 (b)), drain current significantly decrease due to the potential barrier under the gate sidewall. Therefore, source regions should be aligned at the gate edge (Fig. 5 (c)). Process sequence of self-aligned Btm-S TFET is shown in figure 6. First, blanket implanted Btm-S and epitaxial channel layer were formed in the active area. Next, after the formation of gate stacks, source and drain regions were recessed by RIE with SiN gate hard-mask and offset spacer. Then, all of the bottom source regions outside of the gate region are etched in order not to create potential barrier. Finally, epitaxial silicon (Epi-Si) was grown on the etched regions; then, ion implantation for source and drain regions were carried out followed by activation process of 1000 °C RTA.

ii) *Steeper tunneling junction formation.*

S.S. in nTFET is generally worse than that in pTFET due to the broad boron profile in tunneling junction. Improvement of device property in nTFET is indispensable to realize complementally TFET. Since tunnel junction in self-aligned Btm-S TFET is formed before the formation of gate stack and S/D activation annealing, suppression of the impurity diffusion in tunneling junctions is the key. Selective epitaxial growth scheme was utilized to control the dopant profile in tunnel junction. Three types of tunnel junctions were formed.

Type I: Carbon doped Si (Si:C) + i-Si (10 nm)
Type II: Phosphorus-doped-Si (Si:P) (10 nm)
Type III: Si:C + Si:P (10nm)

Device characteristics of fabricated Btm-S TFET

I_D-V_G characteristics applied with various types of tunnel junctions are shown in figure 7. Doping profiles in those samples were confirmed by SIMS analysis (Fig. 8: type I. Fig. 9: type II. Fig. 10: type III). When compared with type I (Si:C + Si) and type III (Si:C + Si:P), it was observed that phosphorus doping reduces V_{TH}. This is explained by the opposite type of doping formation on channel surface (Fig. 8 and 10); also, higher electric field is formed at tunnel junctions. If type II (Si:P) and type III (Si:C + Si:P) are compared, even lowered V_{TH} was achieved by the formation of Si:C layers between boron doped regions and Si:P regions. Figure 9 and 10 indicate that Si:C layers suppress the diffusion of doped boron and creates steeper tunnel junction. Higher electric field in tunnel junctions in type III (Si:C + Si:P) reduces V_{TH} and S.S., and improves current drive-ability. Based on these results, P-N tunnel junction formation by opposite type of doping and the application of diffusion barrier layers of Si:C are indispensable to realize steeper tunnel junction formation in Btm-S TFET.

Consideraton of V_{TH} variability and scalability in Btm-S TFET

Proposed self-aligned Btm-S TFET with "Si:C + Si:P" layers indicates suppressed variability in I_D-V_G characteristic (Fig. 11). Tight V_{TH} distribution in proposed self-aligned Btm-S TFET was experimentally confirmed (Fig. 12) as expected in figure 4. In general, I_{OFF} should increase with L_G scaling shown in figure 1; however, I_{OFF} could be reduced in self-aligned Btm-S TFET with the same I_{ON} / I_{OFF} ratio (Fig. 13). This indicates that I_{OFF} could be scalable in TFET scaling, and proposed TFETs are promising approach to achieve ultra low power applications.

Conclusion

We demonstrated self-aligned Btm-S TFET with epitaxial growth layers of "Si:C + Si:P". It was confirmed that uniform vertical direction tunneling current suppresses V_{TH} variability. Self-aligned Btm-S TFET achieves lowered I_{OFF} with L_G scaling, indicating that proposed TFET is advantageous for ultra low power applications.

Reference

[1] T. Mori, etal., Jpn. J. Appl. Phys. 50 (2011) 06GF14 [2] Y. Kondo et al., SSDM (2013) pp. 746 [3] Y. Morita, et al. SSDM pp.801-802, (2012) [4] A. M. Walke et al., IEEE TED 60(2013) pp.4065

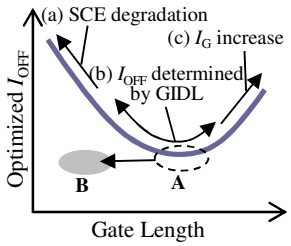

Fig. 1: Schematic image of I_{OFF} dilemma in conventional MOSFET. Minimal I_{OFF} is determined by (a) SCE, (b)I_G, and (c) GIDL.

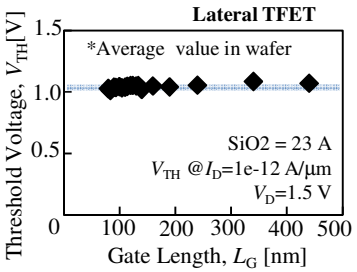

Fig. 2 V_{TH} roll-off behavior of lateral TFETs. Suppressed V_{TH} roll-off is confirmed. Since tunneling current occurred at gate edge, device characteristics are independent of L_G

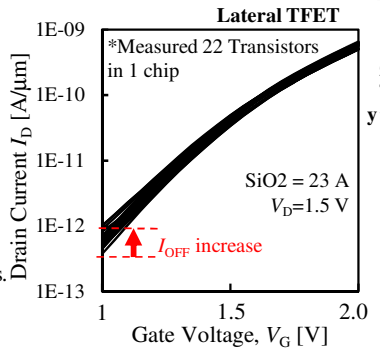

Fig. 3 I_D-V_G characteristics in lateral TFETs. I_{OFF} increase by V_{TH} variability degradation was observed. Lateral TFET is not appropriate to adopt for ultra low leak application.

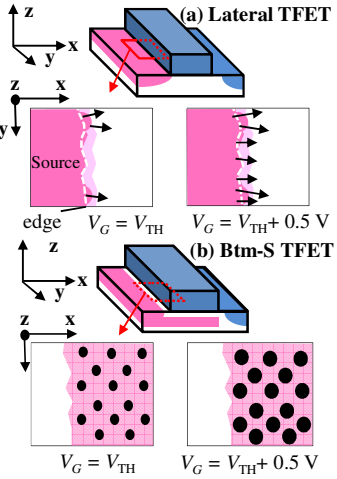

Fig. 4: Schematic images of TFET operation. (a) Lateral TFET (b).Btm-S TFET

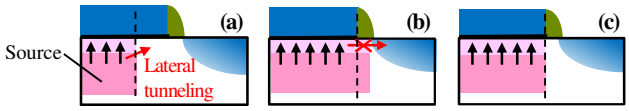

Fig. 5: Btm-S TFET operation in various drain engineering. (a) source regions are formed inside of gate electrode. (b) source regions are extended from the gate edge. (c) source regions are aligned at the gate edge.

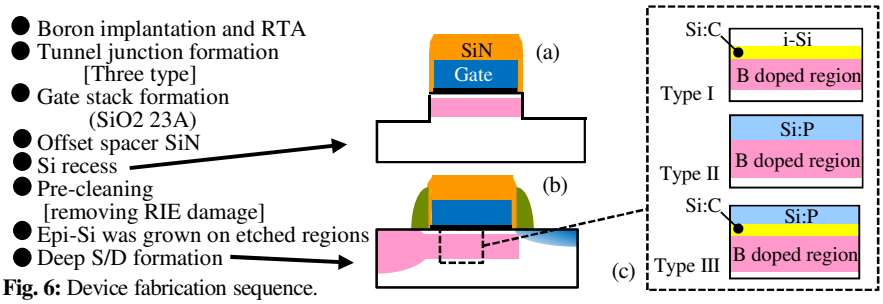

Fig. 6: Device fabrication sequence. (a) Schematic image of Si recess. Tunneling areas are restricted by self aligned process. (b) TFET after source and drain formation. (c) Evaluated three types of tunnel junction. Type I Carbon doped Si (Si:C) + i-Si layer. Type II Phosphorus doped Si (Si:P) epitaxial layer. Type III Si:C epitaxial layer + Si:P epitaxial layer. Carbon concentration in Si:C layer was 2.0%

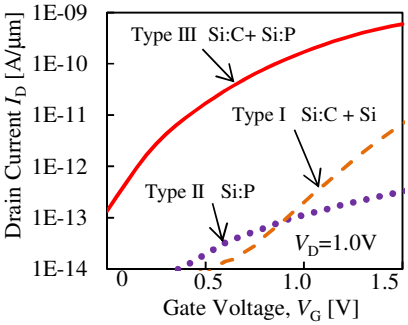

Fig. 7: I_D-V_G characteristics of three types of TFETs. Steep tunnel junction formation was observed in type III, indicating the lowed V_{TH} and S.S.

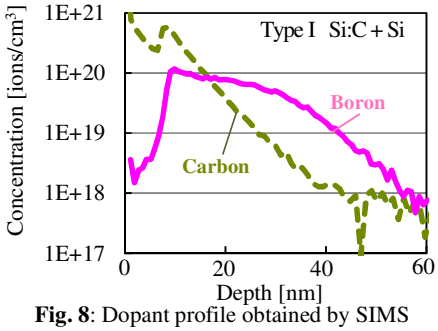

Fig. 8: Dopant profile obtained by SIMS analysis (Type I). Si:C layers suppresses boron diffusion to the channel serface

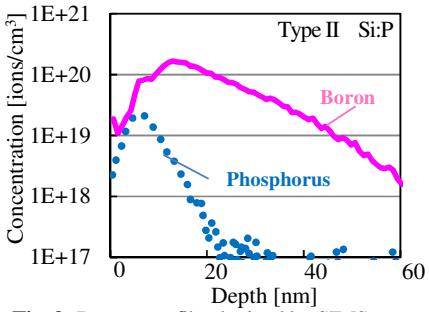

Fig. 9: Dopant profile obtained by SIMS analysis (Type II). Phosphors are doped at channel surface. Boron diffuses to the surface

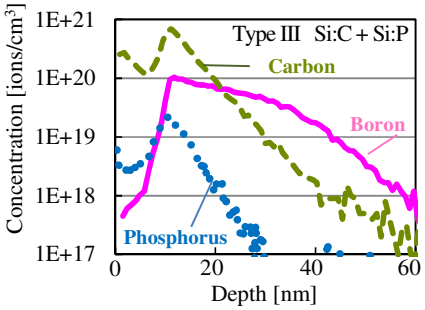

Fig. 10: Dopant profile obtained by SIMS analysis (Type III). Suppressed boron diffusion by Si:C layers are confirmed.

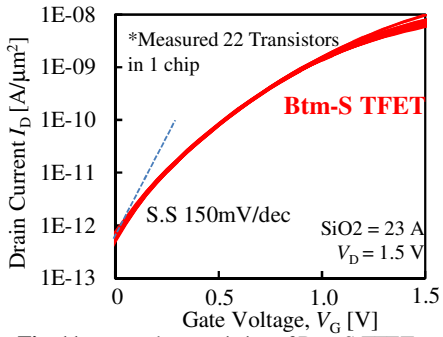

Fig. 11: I_D-V_G characteristics of Btm-S TFET. Suppressed variability in device characteristics was achieved in proposed TFET due to the areal tunnel current under gate electrode

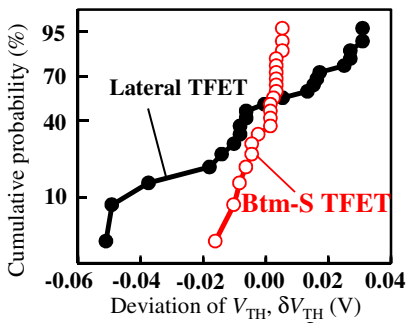

Fig. 12: Cumulative probability of δV_{TH} in lateral TFET (in Fig. 3) and BtmS TFET (in Fig. 11) . Tight V_{TH} variability of BtmS TFET was successfully confirmed than lateral TFET.

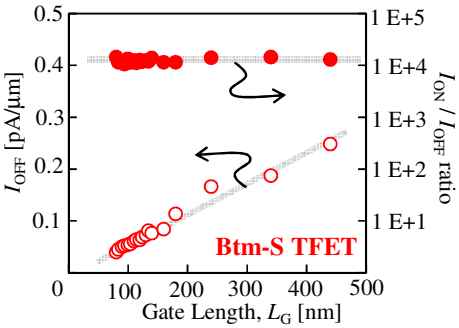

Fig. 13: I_{OFF} decrease and I_{ON} / I_{OFF} ratio (@V_G = 1.5 V / 0.0 V) with L_G scaling. Conventional MOSFET shows difference tendency.