Fabrication Process and Thermal Stability of Isoelectronic Traps for High ON-current Si-based Tunnel Field-Effect Transistors

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Abstract

It was recently reported that the Al-N isoelectronic trap (IET) technology can enhance ON current of Si-based Tunnel Field-Effect Transistors (TFETs). In this paper, we describe the IET-fabrication process in detail and address an issue of thermal budget. We demonstrate that a complex of Al and N atoms plays a key role in the enhancement of the tunnel current. The Al-N IET are not able to survive a rapid annealing at 1000°C, mainly due to desorption of N atoms.

1. Introduction

The tunnel field-effect transistor (TFET) is a promising candidate to realize much steeper switching with the subthreshold swing (SS) less than 60 mV/decade, which is a fundamental switching limit of conventional metal-oxide-semiconductor FETs (MOSFETs) at room temperature. Although steep switching of Si-based TFETs has been demonstrated [1], the high barrier resistivity of the source-channel tunnel junction prevents from boosting the ON current. Therefore, new channel materials, Ge, III-V, and so on, have been introduced into the TFETs [2]. On the other hand, recently, the authors proposed a new tunnel



Fig. 1 (Upper) A schematic and a TEM picture of SOI-TFETs. (Lower Left) The device fabrication process flow. (Lower Right) PL spectra at 10 K, which indicates that the Al-N IETs have been successfully introduced in the Si channel.

current boosting technology in which Al-N isoelectronic traps (IETs) are introduced into the Si channel, and demonstrated the ON current enhancement of silicon-on-insulator (SOI)-TFETs [3]. This previous result suggests that pseudo-direct transition was achieved in the Si tunneling junction by the IETs. In this study, we discuss the formation of Al-N IETs in Si-channels in detail, and point out the thermal budget issue.

2. Experimental

The schematic illustration and TEM image of the fabricated N-type SOI-TFET are shown in Fig. 1. The IETs were formed by ion implantation (I/I) of Al and N and low temperature (LT) annealing at 450°C in nitrogen atmosphere for 60 hours [4]. Finally, the HfO₂/SiO₂ gate stack structures were fabricated, for which the equivalent-oxide-thickness was estimated to be about 1.0 nm.

The Al-N IET transition centers were identified by low temperature photoluminescence (PL) measurements, as also shown in Fig. 1. The reference Si sample shows TA phonon emission. It is noted that TA phonon is responsible for the indirect tunneling of Si p-n junction [5]. However, the Al-N IET-induced Si sample shows stronger IET peak, indicating the higher IET transition probability.

3. Results and Discussion

The SIMS profiles of Al and N for before and after the LT annealing shown in Fig. 2 reveal that the diffusion of these atoms during the annealing is limited to be less than a few nm. On the other hand, the PL spectra show dramatic



Fig. 2 (Left) SIMS profiles for Al and N I/I with the energy of 15 keV and the dosage of 5×10^{13} cm⁻². The 60 hours LT annealing process makes no change of the profiles. (Right) PL spectra for various samples varying the Al and N dosage.



Fig. 3 (Left) Elevated temperature I-V characteristic of an Al-N implanted epitaxial diode. (right) Arrhenius plot of the current at -2.0 V.

change after the LT annealing, which indicate the formation of IETs. These results suggest that the IET formation takes place due to the atomic-scale movement of Al and N atoms in Si. In addition, the PL spectra in Fig. 2 show that the amount of IET centers increases with increasing implanted Al and N does from 5×10^{11} to 5×10^{12} cm⁻², but does not change largely by increasing dose from 5×10^{12} cm⁻² to 5×10^{13} cm⁻². Thus, the optimum dose is expected to be around 10^{13} cm⁻².

The p-n diodes were used to explore the effect of IETs on the electrical characteristics, as the temperature dependence of I-V curves shown in Fig. 3. The Arrhenius plot of the current at -2 V are shown in Fig. 3, which has two temperature ranges, *i.e.*, temperature-sensitive and temperature-insensitive ranges. Since the former behavior is roughly attributed to trap-assisted tunneling, we focus on the low-temperature range. It is obvious that the introduction of Al-N IETs results in the increase of temperature-insensitive tunneling, suggesting that pseudo-direct transition was achieved. On the other hand, we cannot find the current enhancement for the implantation with only N. The current enhancement for the implantation with only Al is not so large either, compared with the Al-N implantation. Thus, we concluded that Al-N complex acts as an IET center.

The I_D - V_G curves of fabricated SOI-TFETs shown in Fig. 4 exhibit that the ON-current of Al-N IET-assisted device is about 10 times higher than that of the reference device. This suggests that the IET technology successfully enhances the ON current of TFET. However, the ON current decreases after the RTA at 1000°C, suggesting that the Al-N IET centers cannot survive in such higher temperature process. Actually, IET peaks in the PL spectrum completely disappear after the RTA [Fig. 4]. The SIMS profile exhibits that N atoms desorbed after the RTA [Fig. 4]. We should note that Si channel of the actual SOI-TFET is thinner than the length of this N diffusion. In this work, we employed low temperature gate stack process (~500°C) after the IET formation, in order to suppress the thermal effect on the IET characteristics. However, the high temperature oxidation process is generally required to suppress the interface state density, which is important to achieve the steeper SS switching. Thus, the thermal tolerance of the



Fig. 4 (Upper) I_D - V_G curves of the fabricated SOI-TFETs. The IET-assisted TFET has about 10 times higher ON current than the reference TFET. However, a higher temperature RTA process (1000°C, 1s) following the IET formation diminishes the advantage of the IET. (Lower left) PL spectra at 20 K. The IET centers disappear by the HT annealing. (Lower right) SIMS profile for Al and N after the high temperature RTA, which exhibits the desorption of N atoms.

IET centers is regarded to be one of the key issues in the development of IET-TFETs.

4. Summary

Our Al-N IET fabrication process successfully achieved ON-current enhancement for the SOI-TFET, presumably due to the effect of the pseudo-direct transition. However, the Al-N IETs are not able to survive in high temperature processes. We proposed that further engineering is required to fabricate more tolerant IET-tunnel junction.

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