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Comprehensive Investigation of Self-Heating Effect (SHE) in Nanoscale Planar and Fin FETs: Impacts of Device Parameters on SHE and Analog Performance Optimization

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Introduction

FinFETs have been utilized for the mass-production of the 22-nm node [1]. As another candidate for beyond the 22-nm node, ultra-thin (UT) BOX SOI FETs have attracted growing interests [2]. Although the electrostatics of these devices is superior, device temperatures (T_{dev}) under operations are generally higher than that of conventional planar bulk devices [3-5]. The increase in T_{dev} (ΔT_{dev}) is originated in the low thermal conductivity of SiO_2; self-heating effect (SHE). Since ΔT_{dev} might cause performance degradations and reliability issues, LSIs must be designed to suppress SHE. However, the impacts of various device parameters on SHE and performance degradations due to SHE have not been thoroughly studied.

In this work, the SHE of nanoscale planar and Fin FETs are comprehensively investigated. For planar FETs, ΔT_{dev} in bulk and SOI FETs with various SOI and BOX thicknesses (t_{SOI}, t_{BOX}) are experimentally extracted. For FinFETs, SHE impacts on analog performances are evaluated for bulk and SOI FinFETs.

Self-Heating Effect (SHE) in Planar FETs

A. Experiments

SHEs in bulk and SOI FETs with a wide variety of t_{SOI} and t_{BOX} (Table I), including the 6-nm UT BOX device (Fig. 1), are evaluated. The T_{dev}'s of bulk and SOI FETs are extracted using the four-terminal (4-T) gate resistance technique [5]. ΔT_{dev} is detected with excellent accuracy within 5 K due to the high temperature dependence of electrical resistance in NiSi/poly-Si gate electrodes [6].

B. Bulk FETs

So far, the SHE of conventional planar bulk FETs has been considered to be negligible. However, a clear increase in T_{dev} is observed in 4-T gate resistance measurements (Fig. 2). In order to investigate the origins of SHE in bulk FETs, thermal resistance (R_{th}) is introduced as a slope of the characteristic curve, which corresponds to the magnitude of SHE.

As shown in Fig. 3, R_{th} increases as L_g decreases, indicating that SHE is stronger in scaled devices. The L_g dependence of R_{th} implies that the SHE of bulk FETs originates from a decrease in the thermal conductivity of a heavily doped well λ_{well} (Fig. 4) [7]. Since the well region resides in the dominant heat dissipation path, λ_{well} has a considerable influence on the T_{dev} of bulk FETs. In shorter L_g devices, well doping becomes higher owing to the overlap of halo implantations, resulting in an increase in R_{th}.

C. SOI FETs

The SHE of SOI FETs is strongly affected by t_{BOX} and t_{SOI}. Although the T_{dev} of thick BOX SOI FETs is much higher than that of bulk FETs, the T_{dev} of SOI FETs can be reduced by thinning the BOX. A smaller R_{th} in thin BOX devices is observed in the entire L_g region (Fig. 5), indicating that BOX thinning is effective even in deeply scaled devices. On the other hand, R_{th} increases in thinner SOI devices (Fig. 6) because of reduced thermal conductivity in thinner layer Si (Fig. 4) [8].

D. Comparison between bulk and SOI structures

Fig. 7 shows $\Delta T_{dev,SOI}/\Delta T_{dev,bulk}$, namely the ratio of ΔT_{dev}'s for the short-channel bulk and SOI FETs, as a function of t_{BOX}. As t_{BOX} decreases, $\Delta T_{dev,SOI}$ is closer to $\Delta T_{dev,bulk}$. In the 6-nm UT BOX devices, the ΔT_{dev} of SOI FETs is almost comparable to that of the bulk FETs. Furthermore, at an elevated chip temperature (T_{chip}), $\Delta T_{dev,SOI}/\Delta T_{dev,bulk}$ decreases owing to the larger temperature dependence of R_{th} in bulk FETs [6].

Self-Heating Effect (SHE) in FinFETs

A. Simulation method

Lattice temperature (T_L) and electrical characteristics are calculated using device simulator by Synopsys Inc. [9]. Device parameters are tuned to satisfy the requirements for 14-nm node [10]. The degradations of thermal conductivity in doped or thinner layer Si are incorporated.

B. Analog performance optimization

Figs. 8 and 9 show the T_L of bulk and 5-nm UT BOX SOI FinFETs under a DC bias corresponding to analog operations. The analog operation T_{dev} of UT BOX SOI FinFETs is much smaller than that of bulk FinFETs. However, such an extremely thin BOX structure might increase parasitic capacitances (C_{para}) which causes performance degradations.

In order to investigate SHE impacts on analog performance, t_{BOX} dependences of the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are evaluated. It is clearly observed that the f_T and f_{max} of SOI FinFETs mark the peak at t_{BOX} of around 10 nm (Fig. 10). The frequency peaks result from the combination of R_{th} increase in larger t_{BOX} and C_{para} increase in smaller t_{BOX}. Thus, the analog performances of SOI FinFETs can be maximized by optimizing t_{BOX} in terms of electrical and thermal properties.

Furthermore, the thermal-aware device design is also effective for low power operations. By thinning the BOX, f_T increases in the entire bias voltage range, indicating that analog operation voltages of UT BOX devices can be suppressed without performance degradations (Fig. 11). In the case of 14-nm node 10-nm UT BOX SOI FETs, both V_d and V_g are reduced by 0.1 V at the same f_T of around 3 THz. As a result of the bias voltage reduction, analog power consumption decreases by around 70%, indicating a great impact of thermal managements on low power operations.

Conclusions

The self-heating effect (SHE) of nanoscale planar and Fin FETs are comprehensively investigated. For conventional planar bulk FETs, it has been verified that SHE is not negligible in nanoscale devices owing to the decrease in λ_{well}. For both planar and Fin FETs, ultra-thin BOX structures are effective to suppress SHE. Particular for SOI FinFETs, the higher analog performance and lower T_{dev} than those of bulk FinFETs can be achieved by optimizing t_{BOX}. Furthermore, the BOX thinning is also effective for the reduction of analog operating voltages. In 14-nm node SOI FinFETs, it is demonstrated that analog power consumption is decreased by around 70% by thinning the BOX.

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References

[1] C. Auth *et al.*, Dig. Symp. VLSI Tech., p131, 2012.
[2] Y. Yamamoto *et al.*, Dig. Symp. VLSI Tech., p212, 2013.
[3] T. Takahashi *et al.*, IEDM Tech. Dig., p809, 2011.
[4] M. Shrivastava *et al.*, IEEE Trans. Electron Devices, **59**, p1353, 2012.
[5] L. T. Su *et al.*, IEEE Trans. Electron Devices, **41**, p69, 1994.
[6] T. Takahashi *et al.*, IEDM Tech. Dig., 7.4.1, 2013.
[7] M. Asheghi *et al.*, J. Appl. Phys., **91**, p5079, 2002.
[8] W. Liu *et al.*, IEEE Trans. Electron Devices, **53**, p1868, 2006.
[9] Sentaurus: http://www.synopsys.com/
[10] T. Takahashi *et al.*, Jpn. J. Appl. Phys., **52**, p04CC03, 2013.
[11] T. Takahashi *et al.*, Jpn. J. Appl. Phys., **52**, p064203, 2013.

Table I: SOI and BOX thicknesses (t_{SOI}, t_{BOX}) of measured devices.

Substrate	t_{SOI} (nm)	t_{BOX} (nm)
Bulk	–	–
SOI	40	6
SOI	52	21
SOI	52	147
SOI	79	145

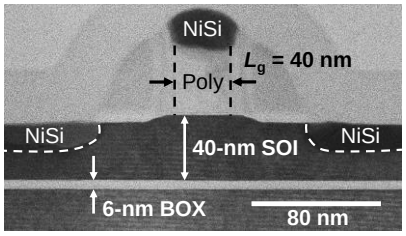

Fig. 1: Cross-sectional TEM image of 6-nm ultra-thin (UT) BOX SOI FETs.

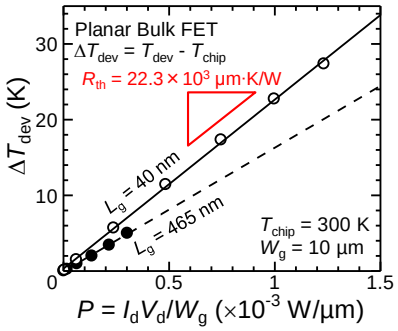

Fig. 2: T_{dev} increase ($\Delta T_{dev} = T_{dev} - T_{chip}$) vs. input power normalized by gate width (P) obtained by 4-T gate resistance technique. T_{dev} is clearly increased, particularly for the shorter gate length (L_g) device, indicating that SHE is not negligible even in bulk FETs.

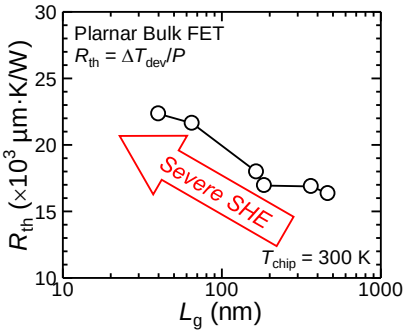

Fig. 3: Thermal resistance (R_{th}) of bulk FETs extracted as the slope of Fig. 2 vs. L_g. R_{th} significantly increases as L_g decreases, meaning that T_{dev} increases in shorter L_g devices.

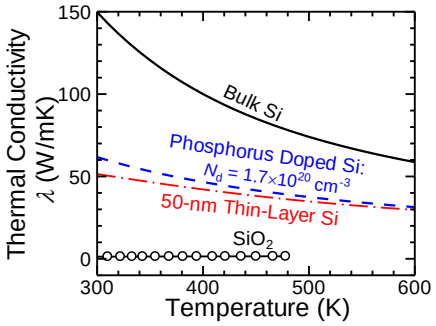

Fig. 4: Temperature dependence of thermal conductivity of Si (λ_{Si}) [7,8] and SiO_2 (λ_{ox}). λ_{Si} is greatly reduced in doped or thin-layer Si. λ_{ox} is much lower than λ_{Si}.

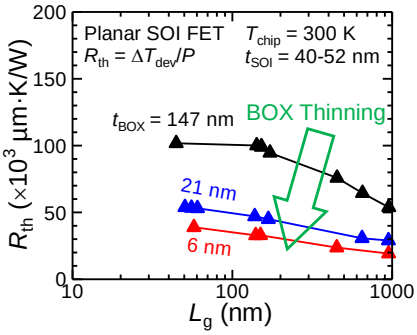

Fig. 5: R_{th} vs. L_g in SOI FETs for various t_{BOX}. The SHE suppression by BOX thinning is observed in the entire L_g region, indicating that BOX thinning is effective even in deeply scaled nodes.

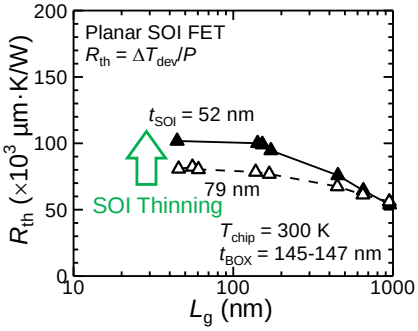

Fig. 6: R_{th} vs. L_g in SOI FETs for various t_{SOI}. SOI thinning has a significant impact on SHE, in particular for shorter L_g devices.

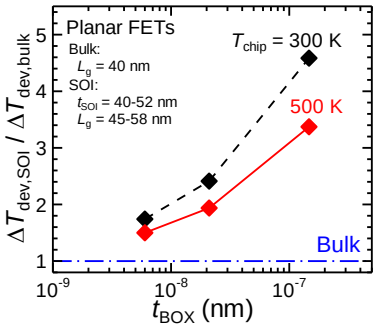

Fig. 7: Ratio of bulk and SOI ΔT_{dev}'s ($\Delta T_{dev,SOI}/\Delta T_{dev,bulk}$) vs. t_{BOX} at T_{chip} of 300 and 500 K. SHE of UT BOX SOI FETs is close to that of bulk FETs. Moreover, the difference becomes smaller at higher T_{chip} owing to the larger temperature dependence of R_{th} in bulk FETs [6].

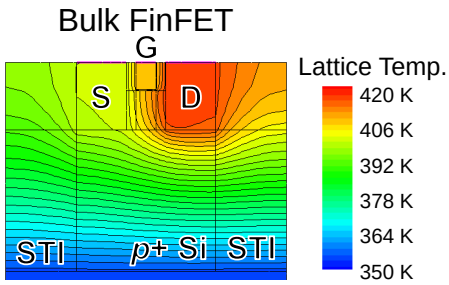

Fig. 8: Contour plots of lattice temperature (T_L) for bulk FinFETs under analog operation (V_g = 0.5 V and V_d = 0.3 V).

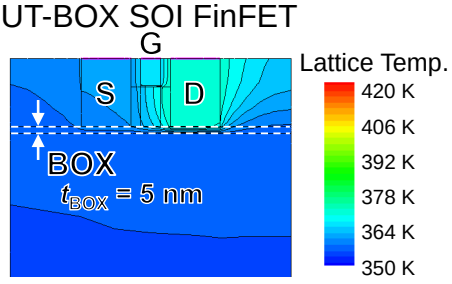

Fig. 9: Contour plots of T_L for UT BOX SOI FinFETs under analog operation (V_g = 0.5 V and V_d = 0.3 V). The analog operation temperature of UT BOX SOI FinFETs is much smaller than that of bulk FinFETs.

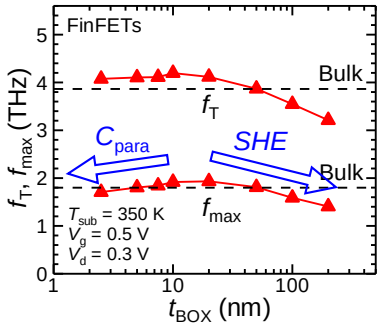

Fig. 10: Cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of SOI FinFETs (triangles) vs t_{BOX}. f_T/f_{max} of bulk FinFETs are also shown (dashed lines).

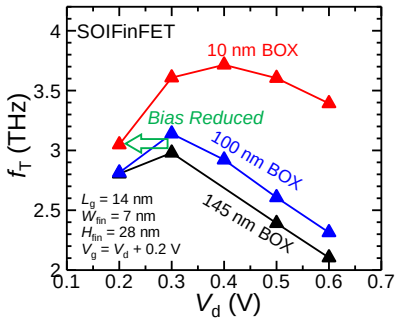

Fig. 11: f_T vs. V_d of SOI FinFETs for t_{BOX} of 10, 100, and 145 nm ($V_g = V_d$ + 0.2 V). By thinning BOX, analog operation voltages can be reduced without performance degradations.