Effective work function shift induced by TiN *sacrificial* metal gates as a function of their thickness and composition in 14nm NMOS devices

C. Suarez-Segovia^{1,2}, P. Caubet¹, V. Joseph¹, O. Gourhant¹, G. Romano¹, F. Domengie¹, G. Ghibaudo²

¹ STMicroelectronics, 850 rue Jean Monnet, 38926, Crolles cedex, France. Phone Number: +33-7-88-22-38-64 Email : carlosaugusto.suarezsegovia@st.com

² IMEP-LAHC, Minatec/INPG, BP 257, 38016 Grenoble, France

Abstract

For the first time, we investigated the effects of composition and thickness of TiN on the effective work function (EWF) shift induced by *sacrificial* gates in 14nm MOS devices with HfON-based dielectrics. No impact of sacrificial TiN composition was observed. Instead, WF was modulated of 35meV by tuning sacrificial TiN thickness. This shift is attributed to the presence of dipoles and/or fixed charges at the IL/HK interface.

1. Introduction

The continuous scaling of MOS transistors makes it imperative to replace the conventional SiO₂/Poly-Si with HKMG stack [1]. A typical high-k metal gate (HKMG) stack structure contains a silicon oxide based interfacial layer (IL), a high-k dielectric, followed by a final metal gate electrode. Generally, band edge metal gates are needed to obtain low threshold voltage (Vth). However, measurements performed on the processed gate stacks show undesirable flat band voltage (Vfb) shifts. This can be attributed to one or several potential drops within the gate stack. As already reported by Jha et al [2], the voltage drops in the insulator at the flat band condition has two origins. The first one is related to the fixed charges, which induces voltage drops increasing linearly with the distance from the gate. The second origin is related to the dipoles at the Si/IL, IL/HK and HK/Metal interfaces. Indeed, according to Iwamoto, Vfb shift in HKMG stacks is mainly determined by the dipole layer at the high-k/SiO₂ interface [3]. Compositional and thickness tuning of the TiN final metal gate film and inclusion of capping layers have recently been studied in order to achieve the desired effective work function in gate-first integration. Nevertheless, HKMG stack engineering can lead to etching issues and serious challenges for gate patterning [4]. To solve this problem, sacrificial gate technique has been recently introduced in advanced 14nm CMOS gate stacks. Thus, the aim of this work is to determine the effective work function shift induced by sacrificial TiN (sac-TiN) metal gates.

2. Extraction of effective work function shift induced by sacrificial metal gates

The CV analysis of MOS devices is widely used for its ability to determine the equivalent oxide thickness (EOT) and the flat band voltage (Vfb) by fitting experimental measurements with quantum simulations [5]. According to Eqs. (1) and (2), EWF depends on metal vacuum work function (WFm) but also on interfacial drops (δV) and on the fixed charges at the IL/HK and Si/IL interfaces.

$$Vfb = EWF - \Phi_{Si}$$
(1)

$$EWF = WFm + \delta V - EOT_{HK} (Q_{SiOX/HK}) - EOT(Q_{Si/SiOX})$$
(2)

The shift in EWF induced by fixed charges depends on the EOT. Therefore, we use the IL-bevel method in order to get rid of this shift. The extrapolation of the curve EWF (EOT) to EOT=0 leads to a typical effective work function (EWF₀), which is characteristic of each HKMG stack without the effect of fixed charges at the IL/Si interface (Q_{Si/SiOx}). Charbonnier demonstrated that the y-intercept is invariable irrespective of the HfO₂ thickness [6]. We can then neglect the contribution of the fixed charges at the IL/HK interface $(Q_{SiOx/HK})$ to the EWF₀. In order to extract the EWF shift induced by sacrificial metal gates, we will apply the IL-bevel method on two types of samples. In the first one, the electrode consists only of the final TiN metal that will serve as a reference. In the other one, we deposit the sacrificial metal gate to be studied, followed by a thermal treatment under N2 atmosphere at 900 °C. The purpose of the stage anneal is to activate the diffusion of elements tuning the work function into the high-k. Next, the metal gate is removed by wet etching, and we deposit the same final TiN metal used as reference.



Fig. 1: a) EWF shift induced by sacrificial gates, b) Sample with only Final TiN, c) Sample with also sacrificial TiN metal gates.

In this way, the EWF₀ obtained with IL-bevel method for samples b) (only final TiN) and samples c) (with sac-TiN) can be expressed as written in Eqs. (3) and (4), respectively. The workfunction shift induced by the sacrificial TiN is therefore determinated using Eq. (5).

$$EWF_{sample 1} = WF_{Final} + \delta_{Final}$$
(3)

$EWF_{sample 2} = WF_{Final} + \delta_{Final} + EWF_{Sac-TiN}$ shift	(4)
$WF_{Sac-TiN}$ shift = EWF _{sample 2} - EWF _{sample 1}	(5)

3. Impact of the composition and thickness of sacrificial **TiN in 14nm NMOS devices**

In this section, we will determine the WF_{shift} induced by TiN sacrificial gate in the context of a 14nm sacrificial gate-first technology as a function of its composition and thickness. Silicon trench isolation (STI) and P-Well were carried out on Si (100) wafers before HKMG stack deposition. Next, 100Å SiO₂ were thermally grown and then wet etched in a circulated HF bath to fabricate the IL-bevel. Standard clean was performed previous to the formation of 10Å eISSG oxide, which is followed by NH₃ nitridation. This last step leads to the SiON which acts as IL layer in the 14nm technology. Fig 2 shows the beveled SiON profile measured by ellipsometry technique. Next, 20Å HfO₂ films were deposited by Atomic Layer Deposition (ALD) followed by Direct Plasma Nitridation (DPN).



Fig. 2: SiON bevel profile measured by ellipsometry.

Then, the set of wafers indicated in Table I were manufactured. The N at-% was measured by X-Ray Fluorescence (XRF) after TiN deposition by Physical Vapor Deposition (PVD). The nitrogen content inside TiN was modified by tuning the argon and nitrogen flow rate during deposition. Devices were completed with the rest of standard Front-End of Line (FEOL) bricks, including Poly-Si deposition, gate patterning, S/D activation anneal and salicide to allow electrical measurements. The electrical measurements were performed on NMOS devices with a gate area of (10 x 10) μ m². C-V measurements were carried out at 100 kHz by using a parametric tester Keithley.

4. Results and Discussion

The EWF-EOT curves obtained for the sample b) and the samples c) in Fig. 1 are shown in Figs. 3 and 4, respectively. EWF_0 for a TiN 35Å is found to be 4.505 eV. From this value, EWF_{Sac-TiN} shifts induced by different sacrificial TiN thicknesses (25Å, 45Å and 85Å) and %N concentration were determined, as indicated in Table I. The sacrificial TiN composition at 45Å seems to have an insignificant effect on WF_{Sac-TiN} shift, contrary to data already reported in the literature (40mV shift on HfO₂ [7] and 200mV shift on HfSiON [8] for the same TiN process variations). In contrast, EWF_{Sac-TiN} shift of 35mV was found by tuning sacrificial TiN thickness between 25Å and 85Å. With the IL-bevel method, we get rid of charges located at the Si/SiON interface.



Fig. 3: EWF-EOT curves for SiON bevel with only final TiN



Fig. 4: EWF-EOT curves for SiON bevel with different sac-TiN thicknesses and compositions.

Table I. EWF shift induced by sac-TiN as a function of its thickness and composition.

Sample	[N ₂]/	N-at%	EWF ₀
	[N ₂]+ [Ar]		(eV)
Only Final TiN	0.5	51.3	4.505
Sac-TiN25Å	0.5	51.3	4.497
Sac-TiN45Å	0.5	51.4	4.502
Sac-TiN45Å-N rich	0.7	52.6	4.502
Sac-TiN45Å-N rich +	1	54.6	4.503
Sac-TiN85Å	0.5	51.6	4.531

Since sacrificial gate is removed, we can neglect the possible TiN/HfON charges induced by the sac-TiN. This shift can therefore only be related to fixed charges and/or dipoles at the HfON/SiON interface induced by the sac-TiN.

5. Conclusions

The shift in EWF induced by different TiN sacrificial gates was accurately determined. No impact of sacrificial TiN composition was observed. Instead, WF of 14nm MOS devices can be modulated of 35meV by tuning sacrificial TiN thickness. This shift is attributed to the presence of dipoles and/or fixed charges at the HfON/SiON interface.

References

- [1] G.D. Wilk, J. Appl. Phys. 89 (2001) 5243
- [2] R. Jha, et al., IEEE Electr. Dev. Lett., 25, 420 (2004)
- [3] K. Iwamoto, et al., Appl. Phys. Lett., 92, 132907 (2008)
- [4] F. Chave et al. 4th Workshop on Plasma Etch and Strip in Microelectronics, (2011)
- [5] C. Leroux et al., MNE 84 (2007) 2408
- [6] M. Charbonnier et al., IEEE T. Electr. Dev. 57 (2010), 1809
- [7] L. Seok-Hee et al., Microelectron. Eng. 109 (2013) 160-162
- [8] S. Baudot, PhD thesis, ed (Université de Grenoble, 2012) 126