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A 16nm FinFET CMOS Technology for Mobile SoC and Computing Applications

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Abstract

A state-of-the-art 16nm CMOS technology is presented. FinFET transistors, 0.07um^2 high density (HD) SRAM, Cu/low-k interconnect and high density MiM de-cap are integrated for mobile SoC and computing applications. This technology provides 2X logic density and >35% speed gain or >55% power reduction over our 28nm HK/MG planar technology. To our knowledge, this is the smallest fully functional 128Mb HD FinFET SRAM (with single fin) test-chip demonstrated with low Vccmin for 16nm node. Low leakage (SVt) FinFET devices achieve excellent short channel control with DIBL of <30 mV/V and superior Idsat of 520/525 uA/um at 0.75V and Ioff of 30 pA/um for NMOS and PMOS, respectively.

Introduction

As CMOS technology continues to advance, FinFET device has been commonly recognized as one of the promising candidates to replace planar device thanks to its excellent electrostatic and short channel control. This paper presents a leading edge FinFET technology for high volume production with optimal process complexity and cost. Competitive SRAM bit cells are designed to provide the optimized standby, cell current and Vccmin. FinFET transistors with multi-Vts are offered to provide design flexibility for wide spectrum applications. High precision resistor, MOS varactors, parasitic BJT and diodes are also offered to enable analog/mixed signal design. Cu/low-k interconnect with different metal combinations of metal thickness and pitch provides balanced R/C and routing density. The planar MiM with high-k dielectric offers high density on-chip capacitor >20fF/um^2 for noise reduction. Key technology features are summarized in Table I.

Process Architecture

Fin patterning and formation on bulk with 48nm fin pitch is realized using pitch-splitting technique where fin width is determined by the sidewall thickness of a mandrel. Poly-silicon deposition and gate patterning on 3-D fin structure is followed by HK/MG RPG process. Raised source/drain with dual epitaxy process is used and optimized to mitigate S/D parasitic resistance. MEOL with W plug provides local routing connected to gate and source/drain. M1 / Mx metal pitch of 64nm is enabled using advanced patterning scheme, whereas single patterning is adopted for metal pitch of 80nm/90nm and above. Cu/low-k process is optimized to have balanced R/C and sufficient manufacturing margin.

Transistor Performance

FinFET transistors with HK/MG are optimized for low power and high performance applications [1]. Figure of Merits (FOM) based on a combination of Inverter, NAND, and NOR with F.O.=3 illustrate >35% speed gain or >55% power reduction over our 28nm HK/MG planar transistors in Fig. 2. Excellent transistor Ion-Ioff characteristics of multi-Vts are shown in Fig. 3 & 4. Both NMOS and PMOS transistors outperform previously reported FinFET and FDSOI transistor data [2-3]. In addition, a benchmark [2-8] on device sub-threshold swing and DIBL is shown in Fig.5, very competitive sub-threshold swing of <65 mV/dec. and DIBL of <30 mV/V are achieved in this work.

FinFET transistors offer excellent analog characteristics. Comparing to 28nm HK/MG planar devices, similar or better 1/f noise characteristics for NMOS and PMOS are reported in [1]. Device mismatch (AVt) reduction by 30% and 25% for NMOS and PMOS, respectively, is achieved as illustrated in Fig.6a. In addition, intrinsic gain (gm/gds) is improved by 3.1X and 2.7X for NMOS and PMOS devices, respectively, as shown in Fig.6b.

SRAM and Interconnect

Competitive HD, HC and HP SRAM cells are designed and optimized for low leakage, high performance and low Vccmin applications. HD/HC SRAM cells provide >70% Isb reduction and >40% speed gain over 28nm HK/MG as shown in Fig.7. The butterfly curves of the 0.07um^2 HD SRAM cell at different voltages are illustrated in [1], where the Static Noise Margin (SNM) of 120mV at 0.6V is obtained. Write assist is validated with 128Mb HD SRAM test-chip with >300mV Vccmin reduction. Fig. 8a &8b show 7-level Cu/low-k metal cross-section view & robust stacked via Rc with tight distribution.

Device and Interconnect Reliability

Gate dielectric quality and process uniformity are keys to improve dielectric breakdown characteristics of FinFET devices. As compared to 28nm HK/MG planar devices, better TDDB MTTF and comparable PMOS NBTI are achieved with careful gate stack process optimization as shown in Fig. 9a &9b. Interconnect reliability passed EM, SM and TDDB spec.. Excellent EM performance of V_x/M_x & V_x/M_{x+1} and SM for 80nm pitch metal is shown in Fig. 10 as an example.

Conclusion

A highly production worthy 16nm FinFET CMOS foundry technology featuring digital & analog functions, dense memory and MiM is presented. Fully functional 128Mb HD SRAM (with single fin) test-chip with high yield and low Vccmin is demonstrated. Overall technology PPA yields >35% speed gain or >55% power reduction over our 28nm HK/MG technology with 2X logic density.

References

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16nm	Technology Features
Process	FinFET, HKMG, Dual-Oxide, Cu/LK
Digital	Core & I/O, multi-Vt
Analog	High-R, Varator, BJT, FMOM
Memory	6T (HD, HC, HP), 2P-8T, DP SRAM, ROM
Chip ID / Repair	Electrical fuse
LC-Tank	Inductor, RF-Varactor, RF-MOM
De-cap	HD-MiM, MOSCAP
ESD	Gated-diode, STI-diode, Snapback MOS

Table. I Summary of 16nm FinFET key technology features.

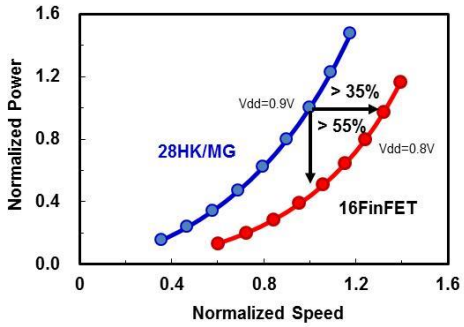

Fig. 2 16nm FinFET provides >35% speed gain or >55% power reduction over 28nm HK/MG planar.

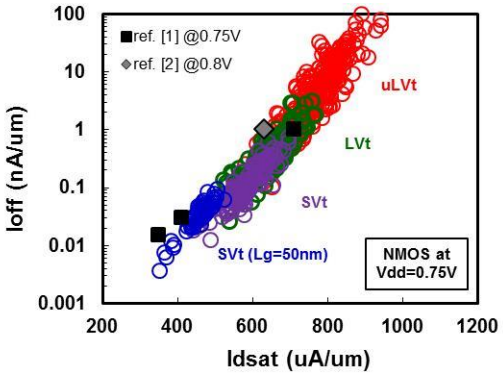

Fig. 3 NMOS Ion-Ioff characteristics of multi-Vt measured at 0.75V & its comparison with that reported in ref.[2-3].

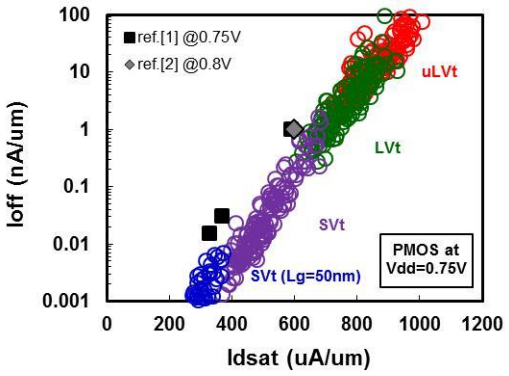

Fig. 4 PMOS Ion-Ioff characteristics of multi-Vt measured at 0.75V & its comparison with that reported in ref.[2-3].

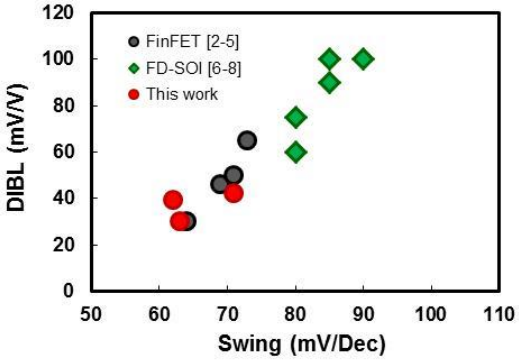

Fig.5 Device sub-threshold swing and DIBL benchmark [2-8].

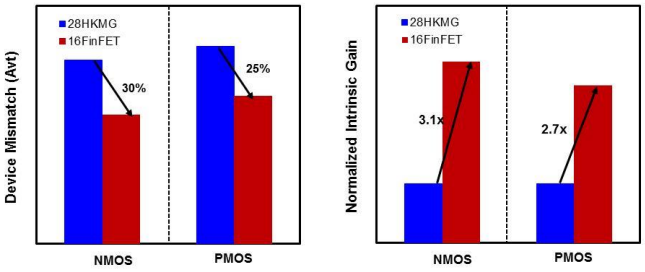

Fig. 6 (a) FinFET devices provide mismatch reduction and (b) higher device gain (gm/gds) than HK/MG planar.

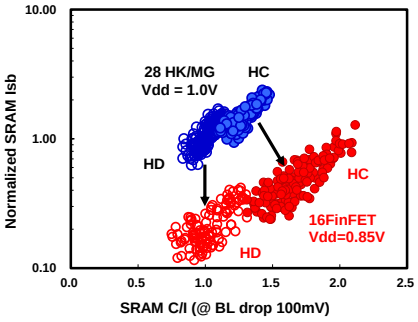

Fig.7 SRAM C/I vs. Isb comparison between FinFET and HK/MG.

Metal	Pitch
M1	1X
M2	1X
M3	1X
M4	1.25X
M5	1.25X
M6	11.25X
M7	11.25X

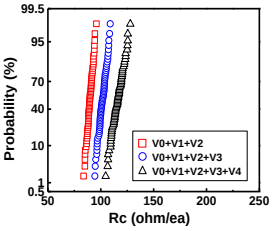

Fig. 8 (a) Cross-section view of Cu/Low for 7-level metal, (b) Cumulative distribution of stacked via R_c resistance.

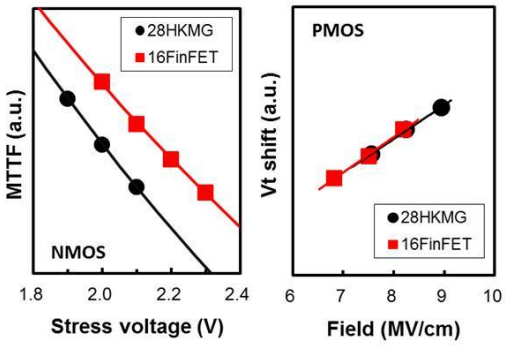

Fig. 9 (a) FinFET device shows better TDDB than 28HKMG and (b) comparable NBTI.

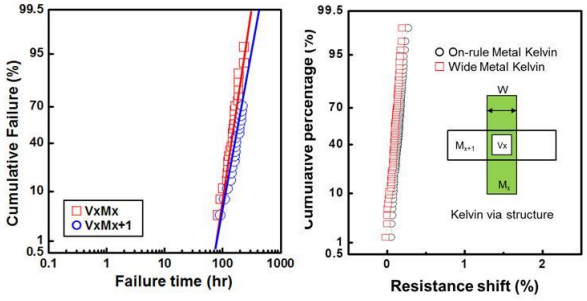

Fig. 10 Robust EM of Vx/Mx and Vx/Mx+1and SM for 80nm metal pitch.