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Detailed Analysis of Minimum Operation Voltage (V_{min}) of Extraordinarily Unstable Cells in Fully Depleted Silicon-on-Thin-BOX (SOTB) 6T-SRAM

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Abstract

The minimum operation voltage (V_{min}) of very unstable cells in silicon-on-thin-BOX (SOTB) 6T SRAM is analyzed in detail. It is found that the worst cell in 16k SRAM happens to be very unstable which corresponds to 6σ from median. It is also found that the unstable cells are very sensitive to V_{TH} change, SNM and V_{min} are well correlated, and a simple V_{TH} variability model is applicable to evaluate cell stability even in very unstable cells.

1. Introduction

The minimum operation voltage (V_{min}) is a key parameter for low voltage operation of large scale SRAM array [1]. However, further V_{min} reduction as well as cell size scaling is becoming more difficult due to increasing random variability of transistors [2-4]. One of the solutions is the introduction of intrinsic channel FD SOI or SOTB FETs that have smaller random V_{TH} variability than bulk FETs [5]. Actually, we have achieved V_{min} of 0.37V in 2M SOTB SRAM [6].

Since V_{min} of large scale SRAM is determined by the worst cell (the most unstable cell) of the array, statistical analysis of cell stability is quite important. The stability of a SRAM cell is usually characterized by SNM. In previous work, we have defined "V_{min} of the cell", and its statistical behaviors have been analyzed [7-9]. However, it has been found that SNM and "V_{min} of a cell" are not necessarily well correlated [7-9].

In this study, "V_{min} of a cell" (hereafter "V_{min}") of 16k intrinsic channel FD SOTB 6T SRAM cells is intensively measured and statistically analyzed. It is found that the worst cell happens to be extraordinarily unstable and its origin is simply V_{TH} variability of each transistor. The behaviors of the very unstable cells are analyzed in detail.

2. Measurements

Device-matrix array (DMA) SRAM TEG [4] with intrinsic channel SOTB FETs was fabricated by the 65nm technology [5-6], where the two storage nodes (VL, VR) are accessible (Fig.1). The SOI thickness is 12nm, BOX thickness is 10nm, and T_{INV} is 2.8nm. In V_{min} measurement, V_{DD} is lowered and V_{min} is defined by V_{DD} where the storage nodes (VL, VR) are flipped. Detailed method is found in Ref. [8].

3. Results

Fig. 2(a) shows measured V_{min} distributions of 16k SOTB SRAM cells. V_{min} deviates from a normal distribution. The worst bit show by far the highest V_{min} of 0.366V. Fig. 2(b) shows measured SNM distributions at V_{DD}=0.4V. It has been known that one-sided SNM follows the normal distribution [4]. However, it is found that the worst 3 bits are deviate from the normal distribution, and a simple extrapolation indicates that the worst cell corresponds to 6σ.

The origin of the extraordinary instability in this worst cell is analyzed in detail. Fig. 3 shows butterfly curves of the worst cell (V_{min}=0.366V). The "eyes" is open at V_{DD}=0.4V while it collapses at 0.3V as expected. Fig. 4(a) shows I-V characteristics of six cell transistors in the worst cell at $|V_{ds}|$=0.4V. pFETs have high V_{TH} while access nFETs have low V_{TH}. In Fig. 4(b-d), V_{THC}'s (defined by constant subthreshold current) in the worst cell are plotted on V_{THC} distributions in 16k SOTB SRAM cells. No abnormality is found and all six transistors are within the normal distribution. Therefore, the origin of the cell instability is simply the V_{THC} variability and the appearance of this extraordinarily unstable cell is just a coincidence.

Fig. 5 shows substrate bias (V_{bs}) dependences of V_{min} and SNM of the worst 3 bits and the median 3 bits at V_{DD}=0.4V. V_{min} decrease and SNM increase as V_{bsn} of nFETs decreases and V_{bsp} of pFETs decreases. Thanks to V_{bsn}=-0.4V, V_{THC} of nFETs is raised and the cell becomes more stable. The eyes becomes open at even V_{DD}=0.3V in the butterfly curve of the worst cell (Fig.6). However, the worst cells are sensitive to V_{TH} change and become unstable more rapidly than the median cells as shown in Fig. 5.

Fig. 7 shows correlation between SNM and V_{min}. Although the poor correlation is found in stable cells, it is found that they are almost perfectly correlated in the unstable cells.

The V_{TH} sensibility analysis of SNM by simulation has been reported [3, 10-11]. In this work, a simple parameter V_{TS} is defined by V_{THC} of transistors in a cell as follows,

$$V_{TS} \equiv Maximum(V_{TaL} - V_{TnL} + V_{TnR} - V_{TpR}, V_{TaR} - V_{TnR} + V_{TnL} - V_{TpL})$$

where V_{THC} of TaL (Fig.1) is expressed as V_{TaL} and so on. Fig. 8 shows correlations between V_{TS} vs. SNM at V_{DD}= 0.4V and V_{TS} vs. V_{min}. In extraordinarily unstable cells, V_{TS} has strong correlation with both SNM and V_{min}, indicating that the cell stability is simply determined by the V_{THC} variability and this parameter is helpful to evaluate cell stability.

4. Conclusions

V_{min} of FD SOTB 6T SRAM cells are intensively measured and statistically analyzed. It is found that the origin of extraordinarily unstable cells is simply V_{THC} variability. It is also found that the unstable cells are very sensitive to V_{THC} change, SNM and V_{min} are well correlated, and a simple V_{THC} variability model applies for cell stability evaluation.

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References

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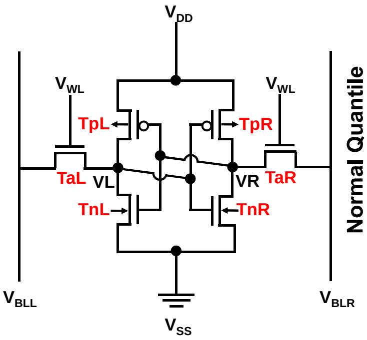

Fig.1. Schematic 6T-SRAM cell.

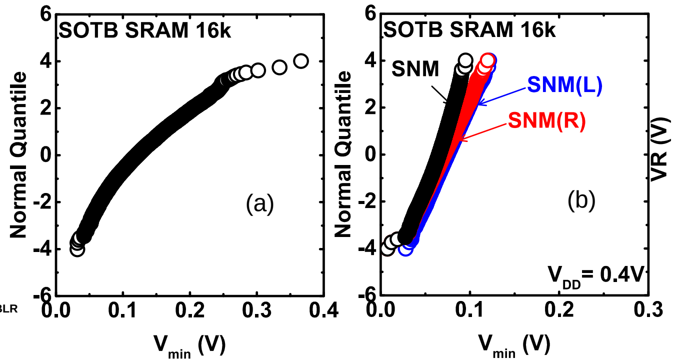

Fig.2. Measured distributions of (a) V_{min} and (b) SNM in 16k FD SOTB SRAM cells.

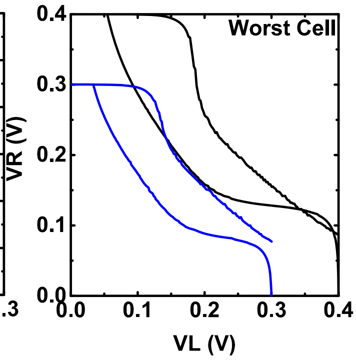

Fig.3. Measured butterfly curves in the worst cell at 0.3V and 0.4V.

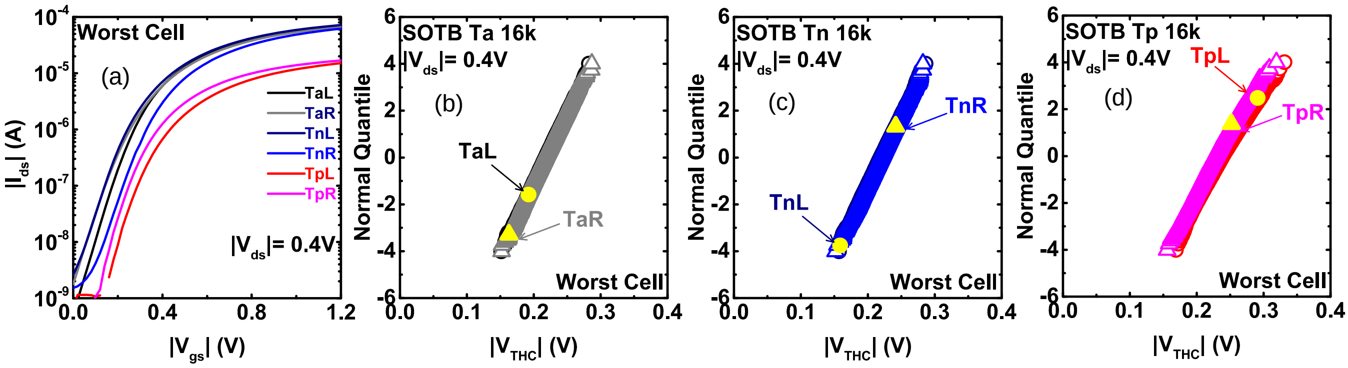

Fig.4. (a) Measured I-V characteristics of 6 cell transistors in the worst cell. V_{THC} distributions of (b) access nMOS (TaL, TaR), (c) driver nMOS (TnL and TnR), and (d) pMOS (TpL, TpR) of 16k FD SOTB SRAM cells. The positions of the worst cell transistors are also plotted in the distributions.

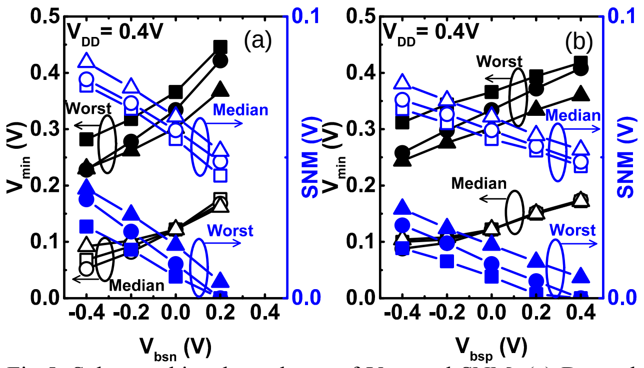

Fig.5. Substrate bias dependence of V_{min} and SNM. (a) Dependence of V_{bsn} of nFETs. (b) Dependence of V_{bsp} of pFETs.

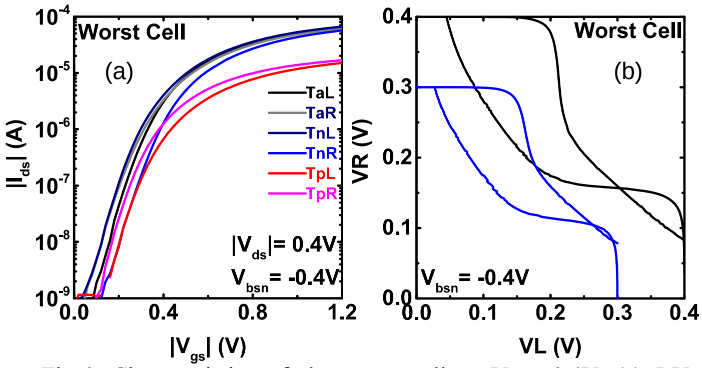

Fig.6. Characteristics of the worst cell at V_{bsn}=-0.4V. (a) I-V curves. (b) butterfly curves. V_{THC} of nMOS is raised and the cell becomes more stable.

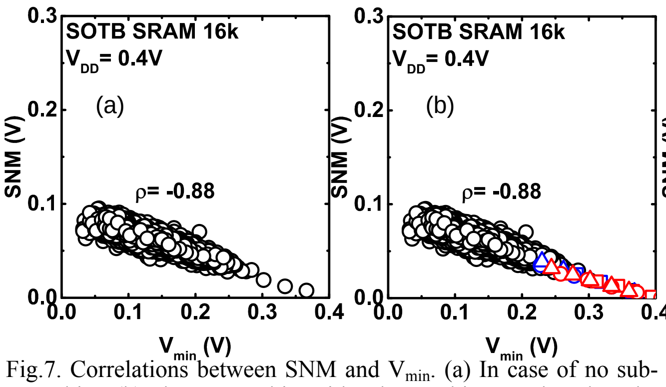

Fig.7. Correlations between SNM and V_{min}. (a) In case of no substrate bias. (b) The worst 3 bits with substrate bias are also plotted.

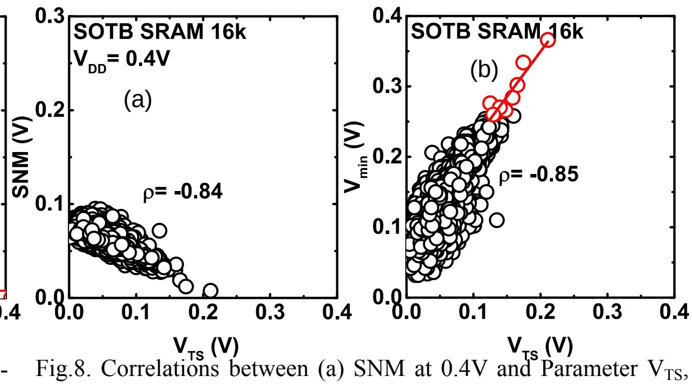

Fig.8. Correlations between (a) SNM at 0.4V and Parameter V_{TS}, and (b) V_{min} and Parameter V_{TS}.