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High Reliability SRAM Development for 40nm Embedded Spilt Gate-MONOS

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Abstract

We found the SRAM failure derived from tailing characteristics of *Vth/Ids* distribution in MCU embedded Split Gate (SG)-MONOS memory. These phenomena can be explained the grain regrowth in poly-Si gate and implanted ions penetration due to thermal budget of SG-MONOS process. Using stacked poly structure for gate electrode, high thermal tolerant SRAM with high affinity to 40nm SG-MONOS was developed.

1. Introduction

Standard MCU product with embedded memory has been to ensure a high yield and reliability by using a mature SOC process. Since current the process generation is progressed beyond 40 nm, various problems have occurred. Especially, Renesas's MCU process chose embedded SG-MONOS [1] added after core/IO device fabrication to keep its reliability. Therefore, thermal tolerance is needed for core/IO devices. In this paper, the device process development with high affinity to embedded SG-MONOS is reported.

2. Thermal budget influence on SRAM characteristics

As shown in Fig.1, the core/IO-device included SRAM fabricates before embedded SG-MONOS in 40nm-MCU products process. In this case, the peripheral devices must be tolerated with the thermal budget of SG-MONOS formation. Using our conventional 40nm logic process, SRAM *Vddmin* shows abnormal characteristics compared without SG-MONOS as shown in Fig.2.

From the variation evaluation with Device Matrix Array (DMA) -TEG, we found there were 3 modes of the *Vth* and *Ids* distribution tail components in this SRAM failure (figure 3(a)-(c)). Figure 4(a)-(c) show physical model explained the above tailing mode. Mode (a) is *Vth* upper tailing and *Ids* lower tailing distribution. This is caused by depleted poly-Si gate covered with large size single grain [2]. To suppress this depletion, an additional annealing was applied after gate doping. However, the abnormal characteristic was still remained in *Vth/Ids* distribution (Fig.3 (b)(c)). Mode (b) is only *Ids* upper tailing distribution and mode (c) is *Vth*/*Ids* lower tailing distribution. Mode (b) is caused by depleted poly-Si gate partially covered with some large size grain. In weak inversion state, small drain current can flow due to partially current path along grain boundary. In fully inversion state, drain current is reduced in proportion to depleted gate area. Therefore, in spite of normal *Vth* distribution, *Ids* distribution is supposed to be lower tailing characteristics. When some grain axis in poly-Si gate aligned with source/drain implantation direction, the implantation ions will be partially penetrated to gate (Fig.4(c)). In this case, since some current paths are partially formed under penetrated region, *Vth* distribution is supposed to be lower tailing characteristics.

From the above data, the origins of these phenomena will come from deterioration of the gate poly-Si by thermal budged during SG-MONOS formation. Therefore, high thermal tolerant poly-Si gate with high affinity to SG-MONOS was needed for the 40nm MCU product.

3. Grain Re-growth Suppression

To suppress grain re-growth, the stacked poly-Si gate structure is chosen. It is enabled to prevent re-growth and channeling during gate implantation. The cross-section picture of stacked poly-Si is shown in figure 5(a). The grain re-growth is stopping in interface between lower and upper layer and grain direction is changed at the interface. The *Vddmin* distribution comparison between single and stacked poly-Si gate is shown in figure 5(b). The *Vddmin* distribution was improved by using stacked poly-Si. Fig.6 shows *Vth* and *Ids* distribution of N/PMOS transistors with stacked poly-Si gate. There was no tail component in *Vth* and *Ids* distribution beyond 4σ. Fig.7 shows frequency difference distribution of ring oscillator between adjacent steps in flip-flop circuit allay with stacked poly-Si and single poly-Si gate. Beyond 5σ, tail components of delta frequency were not given only in case of using stacked poly-Si gate. It is indicated that stacked poly-Si structure is expected for high thermal tolerant device with high affinity to SG-MONOS beyond 5σ.

4. Conclusions

The grain re-growth resulted from thermal history of SG-MONOS formation caused gate depletion and penetration, and degraded SRAM characteristics. To overcome these phenomena, the stacked poly-Si structure applied to 40nm MCU products with SG-MONOS. As a result, we solved this problem and enabled SRAM to be high thermal tolerant.

Acknowledgements

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References

[1] T. Kono et. al., 2013 ISSCC, p212,
[2] Y. Yoshida, et, al., IEDM1999, p475,

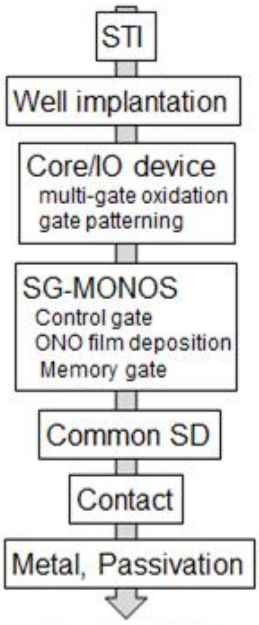

Fig.1 Process flow 40nm-MCU product with SG-MONOS.

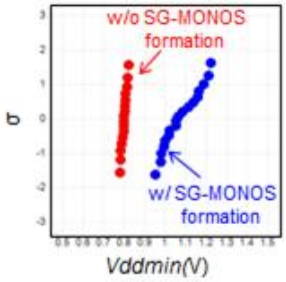

Fig.2 *Vddmin* distribution of SRAM with and without SG-MONOS.

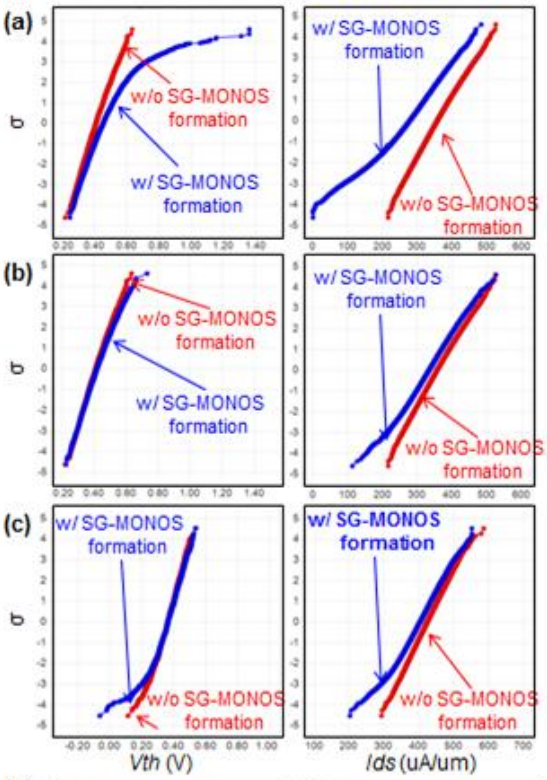

Fig.3 Classified tail component of *Vth* and *Ids* distribution on several SRAM transistor by using decode-type DMA-TEG.

(a)Fully gate depletion mode
(b)Partial gate depletion mode
(c)(b)+partial gate penetrated injection mode

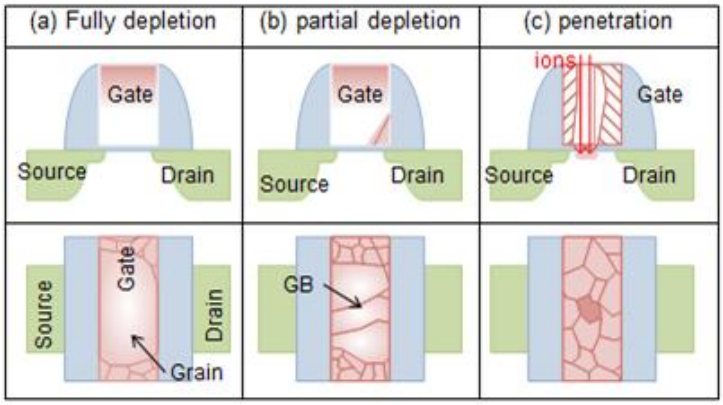

Fig.4 Physical model of several tailing mode.

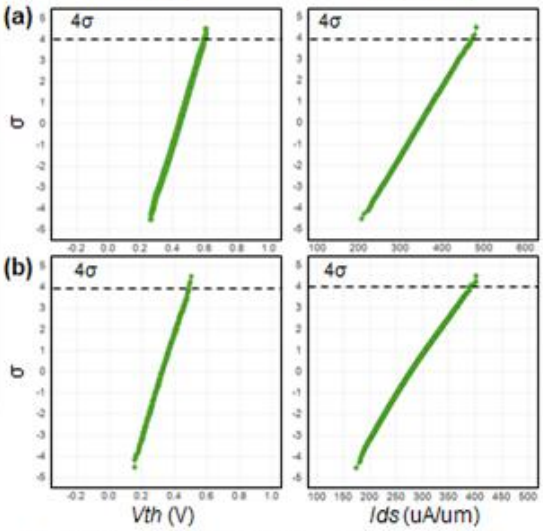

Fig.6 *Vth* and *Ids* distribution of several SRAM transistor by using stacked poly-Si gate. (a)PD device, (b)PU device.

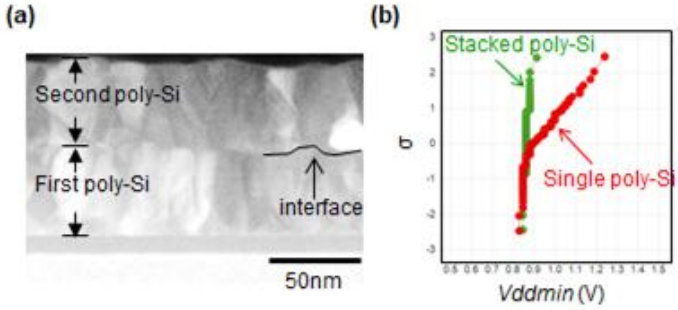

Fig.5 (a) A cross-sectional image of stacked poly-Si and (b) the *Vddmin* characteristics difference between SRAM with stacked and single layer gates.

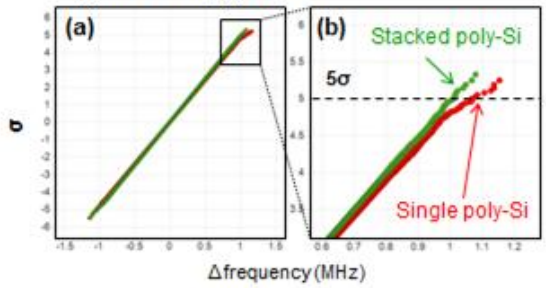

Fig.7 Frequency difference distribution of ring oscillator between adjacent step in flip-flop allay.