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The Guideline of Si/SiGe Hetero-Junction Design in Parallel Plate Style TFETs (PP-TFETs) for Si CMOS Platform Implementation

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Abstract

In this paper, we describe Si-CMOS compatible parallel plate style TFETs (PP-TFETs) with epitaxially grown Si/SiGe hetero-junction. The guideline of optimum Si/SiGe configuration has been theoretically and experimentally proposed for N- and P-type TFETs respectively. With appropriate SiGe application, significantly enhanced ON current and lowered threshold voltage were demonstrated. In addition, novel architecture utilizing Si and SiGe hybrid tunneling region has been proposed. Finally, extremely suppressed OFF current resulting in superior ON/OFF ratio are achieved both in N- and P-type TFETs.

Introduction

Tunneling field-effect transistors (TFETs) have received attention for ultra-low power applications due to its availability of steep sub-threshold slope (*S.S.*) [1]. Si-based TFET enables simple implementation into common Si CMOS platform. Here, SiGe application [2-6] is one of the promising approaches to boost TFET performance owing to its narrower E_g and higher BTBT rate [7], as well as compatibility with common Si-CMOS platform. Also, hetero-junction system was proposed to enhance I_{on} without increasing ambipolar OFF current at drain side [4, 6]. On the other hand, TFET operations with current flow parallel to gate electric field have been proposed to enhance tunneling efficiency [6, 8-10]. PP-TFET [10] is one of the approaches. However, appropriate TFET structure for epitaxially grown SiGe hetero-junction and configuration has not been discussed so far.

In this paper, PP-TFETs are adopted for Si-based TFET and the guideline of Si/SiGe hetero-junctions formation for complimentary TFETs is discussed. Improved I_{on} and controlled V_{th} with avoiding I_{off} increase are demonstrated with optimized Si/SiGe hetero configuration.

Consideration of Si/SiGe configuration in PP-TFETs

Junction formation under gate overlap region determines lateral tunneling currents in conventional TFET (**Fig. 1 (a)**). Meanwhile, parallel plate tunnel junction creates vertical areal currents under gate electrode in PP-TFETs (**Fig. 1 (b)**). This is advantageous not only to increase I_{on} but also to achieve uniform epitaxial growth due to its simple structure for epi-process.

Band diagram of Si and SiGe hetero-structure in N- and P-type TFETs indicates optimum configuration of SiGe layers. In order to enhance ON-state BTBT property, source-SiGe (S-SiGe) for N-TFETs and channel-SiGe (Ch-SiGe) for P-TFETs are preferable (**Fig. 2**). This could be ideal performance booster scheme for Si-based complimentary TFETs (C-TFETs) (**Fig. 3**).

Fabrication of Si/SiGe hetero PP-TFETs

In order to experimentally verify the assumption above, various types of Si/SiGe hetero-tunnel junctions were formed in PP-TFETs (**Fig. 4**). First, for S-SiGe sample, epi-SiGe layer was formed on SOI. Then, source and drain regions were formed by ion implantation technique with activation annealing. Next, for channel-Si (Ch-Si) and Ch-SiGe samples, each epi-channel layer was grown with 3 ~ 6 nm thicknesses. Ge concentration is approximately 38%. After that, very thin Si-cap layers were formed on Ch-SiGe samples followed by gate stack with HfO_2/Al_2O_3 gate dielectrics (EOT = 1.5 nm) and TiN gate electrode formation. Here, source region was extended into under the most of gate region so that gate length (L_g) is almost same as source and gate overlap length (L_{ov}). **Table 1** summarizes each epitaxial condition of fabricated PP-TFETs. Both N- and P-type PP-TFETs were fabricated on the same wafers. **Figure 5** shows high resolution cross sectional transmission electron microscopy (x-TEM) images of fabricated PP-TFETs.

Experimental results and discussion

Appropriate Si/SiGe hetero configuration: **Figure 6** shows I_d-V_g characteristics of N-type TFETs in source-Si (S-Si)/Ch-Si control samples with different L_{ov} (~L_g). I_{on} increases according to L_{ov} increase. This confirms that tunneling currents is vertically generated at tunnel-junction as expected in **figure 1 (b)**. **Figure 7** shows I_d-V_g characteristics of (a) P-type and (b) N-type PP-TFETs with various source and channel materials. In P-TFETs, significant I_{on} improvement and V_{th} lowering are confirmed in S-Si/Ch-SiGe hetero-junction (#3p), compared to S-Si/Ch-Si sample (#1p). However, limited impact is confirmed in S-SiGe/Ch-Si sample (#2p). On the other hand, in N-TFETs, significant advantage of enhanced I_{on} and optimized V_{th} is observed only in S-SiGe/Ch-Si structure (#2n). These behaviors correspond to the previous expectation. This suggests that Si/SiGe hetero-junction in appropriate SiGe configuration is the promising performance booster for Si-based C-TFETs. Furthermore, dramatically enhanced I_{on} and lowered V_{th} are achieved with thicker Ch-SiGe device (#4p) in P-type PP-TFETs (**Fig. 8**). In terms of the current controllability by gate field, thinner epi-ch. could be better [11]. However, the advantage of thicker epi-ch. in this configuration is explained by the contribution of strain effect and weakened quantum confinement effect [6] in the Ch-SiGe layer.

Novel architecture for I_{off} suppression: Although significantly enhanced I_{on} and lowered V_{th} were achieved with appropriate SiGe application, I_{off} was simultaneously increased. This impedes the ultra-low power operation. **Figure 9** shows the dependence of I_d-V_g characteristics on L_{ov} in S-Si/Ch-SiGe samples, indicating no L_{ov} dependency in lower drain current regions. This indicates that parasitic source edge components, which occur at source to gate underlap region, determine I_{off} [6]. The alignment of gate to source edge brings serious trade-off between I_{on} and I_{off} (*S.S.*) degradation. If the source edge extends beyond the gate edge, I_{on} degrades due to potential barrier from the ungated source region. In order to overcome the trade-off, novel architecture with hybrid Si and SiGe tunnel-junction has been proposed for the first time (**Fig. 10**). SiGe layers were patterned by wet etching (SC1 chemistry) so as to underlap to the source edge. This structure enables enhanced vertical tunneling current by Si/SiGe hetero-junction (higher BTBT rate), with suppressing parasitic source edge component by Si/Si homo-junction (lower BTBT rate). **Figure 11** shows I_d-V_g characteristics of fabricated (a) P-type and (b) N-type hybrid Si and SiGe PP-TFETs and conventional Si or SiGe PP-TFETs. Much suppressed I_{off} with improved *S.S.* are successfully demonstrated with hybrid Si and SiGe PP-TFETs. It should be noted that gate leakage current (I_g) are also well suppressed with maintaining relatively thick EOT. This I_{off} level is 3 orders of magnitude lower than that of reported Si/SiGe hetero TFETs so far (**Table 2**).

Conclusion

Si/SiGe hetero PP-TFETs have been widely evaluated in consideration of appropriate SiGe configuration. It was confirmed that SiGe layer must be applied into source region in N-TFET and channel region in P-TFET respectively. Under this guideline, significantly large enhancement of I_{on} and V_{th} shift have been achieved both in P- and N-TFETs. Also, novel architecture with hybrid Si and SiGe PP-TFETs were proposed and demonstrated extremely low I_{off} resulting in prominent I_{on}/I_{off} ratio. This enables the realization of Si-based C-TFETs with current Si CMOS platform for ultra-low power applications.

Acknowledgement

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References [1] L. Wei et al., IEDM (2010) pp. 391., [2] Q.T. Zhao et al., IEEE EDL **32**, NO. 11 (2011) pp1480. [3] A. Villalon VLSI Tech. (2012) pp.49, [4] D. Kim et al., ISLPED (2009) pp. 219., [5] A. Villalon VLSI Tech. (2014) pp.66, [6] A. M. Walke et al., IEEE TED 61 (2014) pp.707, [7] K-H Kao et al., IEEE TED **59** (2012) pp.292., [8] C. Hu et al., IEDM (2010) pp.387., [9] Y. Kondo et al., SSDM (2013) pp. 746. [10] Y. Moria et al., SSDM (2012) pp. 801., [11] P. Patel et al., SISPAD, (2009) pp.23.

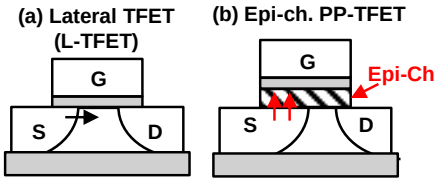

Fig. 1: Schematic diagrams of the structures for (a) lateral TFET and (b) PP-TFET (adopted in this work). Epitaxial channel layer between source and gate is formed in PP-TFET. BTBT parallel to gate electric field is advantageous to enhance gate controllability with increased tunneling area.

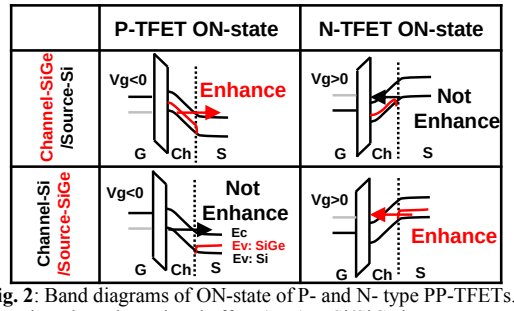

Fig. 2: Band diagrams of ON-state of P- and N- type PP-TFETs. Based on the valence band offset (ΔE_v) at Si/SiGe hetero junction, effective position of SiGe is different between P- and N-type TFETs. Appropriate configuration of SiGe layer is needed to enhance ON-current.

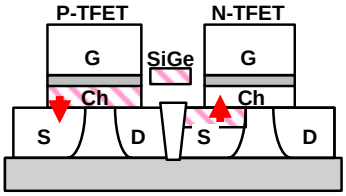

Fig. 3: Ideal structure of complementary Si/SiGe hetero PP-TFET. SiGe application into channel region for P-TFET and source region for N-TFET are preferable to enhance ON-current.

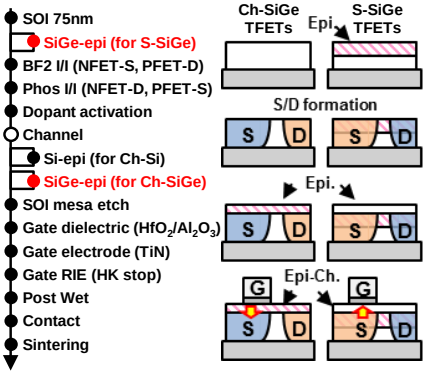

Fig. 4: Process flow of Si/SiGe hetero PP-TFETs. SiGe-epi layers were formed as source or channel material. S/D and gate regions were defined by EB lithography. Source region was extended into under the most of gate region. Drain region is kept away from gate edge by 200 nm to avoid ambipolar OFF-current.

	Source-Epi	Channel-Epi
#1 n/p	None (SOI)	Si 3 nm
#2 n/p	SiGe(38%) 10 nm	Si 3 nm
#3 n/p	None (SOI)	SiGe(38%) 3 nm
#4 n/p	None (SOI)	SiGe(38%) 6 nm

Table. 1: Experimental split condition of source and channel epi-materials. Both N- and P-TFETs were fabricated in the same wafers. Ch-SiGe thickness were varied with 3 and 6 nm. SiGe content of approximately 38% was confirmed by SIMS analysis.

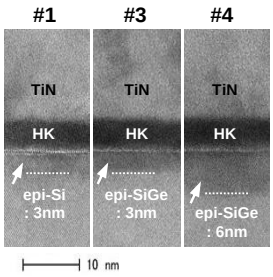

Fig. 5: High resolution x-TEM images of fabricated PP-TFETs. No visible dislocations are seen in all epi-ch layers. This suggests compressive strain is induced in SiGe layer. Note that very thin Si-cap layers on Ch-SiGe were consumed during gate stack and its pre-cleaning process.

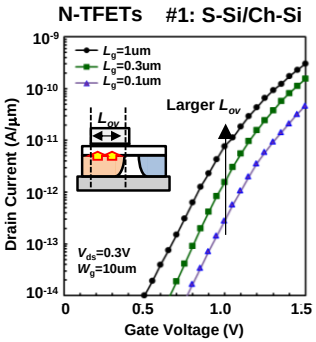

Fig. 6: I_d-V_g characteristics of fabricated control sample of N-type S-Si/Ch-Si PP-TFETs with various L_{ov}. It is confirmed that I_{on} proportionally increases with L_{ov}. This indicates BTBT current in vertical direction is generated under the gate electrode.

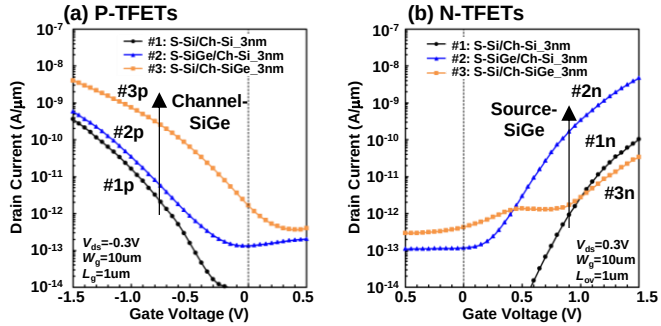

Fig. 7: I_d-V_g characteristics of fabricated PP-TFETs. (a) P-TFETs, (b) N-TFETs. Significant V_{th} reduction and I_{on} enhancement are observed in P-TFET with Ch-SiGe and in N-TFET with S-SiGe. However, opposite types of Si/SiGe hetero samples show limited impact. This confirms appropriate configuration of SiGe application is necessary to boost ON-state current.

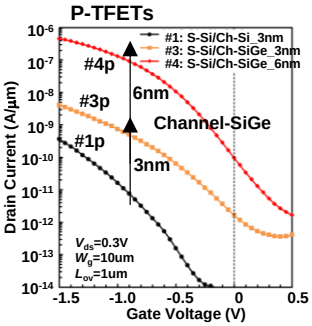

Fig. 8: The dependence of I_d-V_g characteristics on Ch-SiGe thickness in S-Si/Ch-SiGe PTFETs. Remarkable improvement in tunneling property is achieved with thicker Ch-SiGe thickness.

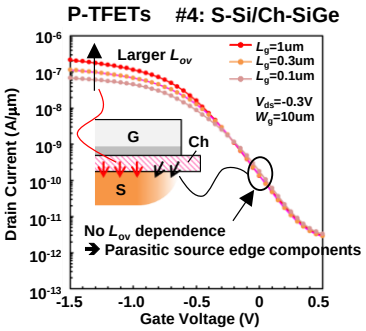

Fig. 9: I_d-V_g characteristics of S-Si/Ch-SiGe in P-TFET with various L_{ov}. I_d (I_{on}) increases with larger L_{ov} in relatively high I_d level. Whereas that is not observed in lower level of I_d (I_{off}). This indicates I_{off} is dominated by not vertical tunneling current but parasitic source edge component.

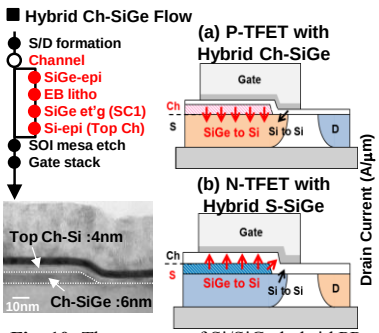

Fig. 10: The concept of Si/SiGe hybrid PP-TFETs. Ch-SiGe or S-SiGe was removed by wet (SC1) patterning process so as to underlap to Si source edge. Only vertical tunneling current is enhanced by Si/SiGe hetero-junction while parasitic tunneling current at source edge in drain side is suppressed by Si/Si homo-junction.

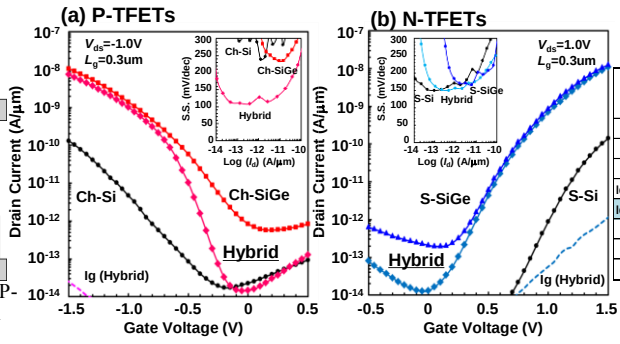

Fig. 11: I_d-V_g characteristics of conventional and hybrid Si/SiGe PP-TFETs. (a) P-TFETs, (b) N-TFETs. By removing SiGe epi-layer with underlapping to source edge, I_{off} is successfully reduced as the same level of I_{off} in Si/Si homo-junction.

	PTFET			NTFET		
	[3]	[5]	This work	[3]	[6]	This work
Structure	Channel-SiGe(30%) L-TFET	Channel-SiGe(25%) NW-TFET	Channel-SiGe(38%) PP-TFET	Channel-SiGe(15%) L-TFET	Source-SiGe(45%) Line-TFET	Source-SiGe(38%) PP-TFET
EOT (nm)	1.25	1.25	1.5	1.25	0.9	1.5
Lg (nm)	200	100	300	200	1000	300
Vd (V)	-1.0	-0.9	-1.0	1.0	0.9	1.0
Ion (uA/um)	6	80	0.002	6	4	0.001
Ioff (uA/um)	4.0E-05	2.0E-05	1.9E-08	3.0E-04	8.0E-05	1.6E-08
Ion/Ioff	1.5E+05	4.0E+06	1.0E+05	2.0E+04	5.0E+04	6.0E+04
SS_min	-	-	107	-	~120	150
SS_ave	133	~100	127	~100	~130	168

Ioff: minimum Id (at Voff) Ion: Id at Vg=Voff+1.0V
SS_ave: SS extracted over 3 orders of magnitudes current from Ioff

Table. 2: Benchmark result of various TFETs with SiGe materials. Hybrid structure of Ch-SiGe or S-SiGe achieved extremely low I_{off} resulting in high I_{on}/I_{off} ratio.