The Guideline of Si/SiGe Hetero-Junction Design in Parallel Plate Style TFETs (PP-TFETs) for Si CMOS Platform Implementation

M. Goto1, Y. Kondo1, Y. Morita1, S. Migita2, A. Hokayazono1, H. Ota1, M. Masahara2, and S. Kawanaka1
1Center for Semiconductor Research & Development, Semiconductor & Storage Products Company, Toshiba Corporation
2Green Nanoelectronics Center (GNC), National Institute of Advanced Industrial Science and Technology (AIST)
Tsukuba, Ibaraki 305-8569, Japan

Abstract
In this paper, we describe Si-CMOS compatible parallel plate style TFETs (PP-TFETs) with epitaxially grown Si/SiGe hetero-junction. The guideline of optimum Si/SiGe configuration has been theoretically and experimentally proposed for N- and P-type TFETs respectively. With appropriate SiGe application, significantly enhanced ON current and lowered threshold voltage were demonstrated. In addition, novel architecture utilizing Si and SiGe hybrid tunneling region has been proposed. Finally, extremely suppressed OFF current resulting in superior ON/OFF ratio are achieved both in N- and P-type TFETs.

Introduction
Tunneling field-effect transistors (TFETs) have received attention for ultra-low power applications due to its availability of steep sub-threshold slope (S.S.) [1]. Si-based TFET enables simple implementation into common Si CMOS platform. Here, SiGe application [2-6] is one of the promising approaches to boost TFET performance owing to its narrow erb and higher BTBT rate [7], as well as compatibility with common Si-CMOS platform. Also, hetero-junction system was proposed to enhance Ion without increasing ambipolar OFF current at drain side [4, 6]. On the other hand, TFET operations with current flow parallel to gate electric field have been proposed to enhance tunneling efficiency [6, 8-10]. PP-TFET [10] is one of the approaches. However, appropriate TFET structure for epitaxially grown SiGe hetero-junction and configuration has not been discussed so far.

In this paper, PP-TFETs are adopted for Si-based TFET and the guideline of Si/SiGe hetero-junctions formation for complimentary TFETs is discussed. Improved Ion and controlled Vth with avoiding Ion increase are demonstrated with optimized Si/SiGe hetero configuration.

Consideration of Si/SiGe configuration in PP-TFETs
Junction formation under gate overlap region determines lateral tunneling currents in conventional TFET (Fig. 1(a)). Meanwhile, parallel plate tunnel junction creates vertical areal currents under gate electrode in PP-TFETs (Fig. 1(b)). This is advantageous not only to increase Ion but also to achieve uniform epitaxial growth due to its simple structure for epi-process.
Band diagram of Si and SiGe hetero-structure in N- and P-type TFETs indicates optimum configuration of SiGe layers. In order to enhance ON-state BTBT property, source-SiGe (Si/SiGe) for N-TFETs and channel-SiGe (Ch-SiGe) for P-TFETs are preferable (Fig. 2). This could be ideal performance booster scheme for Si-based complimentary TFETs (C-TFETs) (Fig. 3).

Fabrication of Si/SiGe hetero PP-TFETs
In order to experimentally verify the assumption above, various types of Si/SiGe hetero-tunnel junctions were formed in PP-TFETs (Fig. 4). First, for S-SiGe sample, epi-SiGe layer was formed on SOI. Then, source and drain regions were formed by ion implantation technique with activation annealing. Next, for channel-Si (Ch-Si) and Ch-SiGe samples, each epi-channel layer was grown with 3~6 nm thicknesses. Ge concentration is approximately 38%. After that, very thin Si-cap layers were formed on Ch-SiGe samples followed by gate stack with HfO2/Al2O3 gate dielectrics (EOT = 1.5 nm) and TiN gate electrode formation. Here, source region was extended into under the most of gate region so that gate length (Lg) is almost same as source and gate overlap length (Lso). Table 1 summarizes each epitaxial condition of fabricated PP-TFETs. Both N- and P-type PP-TFETs were fabricated on the same wafers. Figure 5 shows high resolution cross sectional transmission electron microscopy (x-TEM) images of fabricated PP-TFETs.

Experimental results and discussion
Appropriate Si/SiGe hetero configuration: Figure 6 shows Ioff characteristics of N-type TFETs in source-Si (S-Si)/Ch-Si control samples with different Ion (r ~ r). Ion increases according to Ion increase. This confirms that tunneling currents is vertically generated at tunnel-junction as expected in figure 1(b). Figure 7 shows Ioff characteristics of (a) P-type and (b) N-type PP-TFETs with various source and channel materials. In PP-TFETs, significant Ion improvement and Vth lowering are confirmed in S-Si/Ch-Si hetero-junction (#3p), compared to S-Si/Ch-Si sample (#1p). However, limited impact is confirmed in S-SiGe/Ch-Si sample (#2p). On the other hand, in N-TFETs, significant advantage of enhanced Ion and optimized Vth is observed only in S-SiGe/Ch-Si structure (#2n). These behaviors correspond to the previous expectation. This suggests that Si/SiGe hetero-junction in appropriate SiGe configuration is the promising performance booster for Si-based C-TFETs. Furthermore, dramatically enhanced Ion and lowered Vth are achieved with thicker Ch-SiGe device (#4p) in P-type PP-TFETs (Fig. 8). In terms of the current controllability by gate field, thinner epi-ch. could be better [11]. However, the advantage of thicker epi-ch. in this configuration is explained by the contribution of strain effect and weak quantum confinement effect [6] in the Ch-SiGe layer.

Novel architecture for Ion suppression: Although significantly enhanced Ion and lowered Vth were achieved with appropriate SiGe application, Ion was simultaneously increased. This impedes the ultra-low power operation. Figure 9 shows the dependence of Ion characteristics on Ion in S-Si/Ch-SiGe samples, indicating no Ion dependency in lower drain current regions. This indicates that parasitic source edge components, which occur at source to gate overlap region, determine Ion [6]. The alignment of gate to source edge brings serious trade-off between Ion and Ion (S.S.) degradation. If the source edge extends beyond the gate edge, Ion degrades due to potential barrier from the un gated source region. In order to overcome the trade-off, novel architecture with hybrid Si and SiGe tunnel-junction has been proposed for the first time (Fig. 10). SiGe layers were patterned by wet etching (SC1 chemistry) so as to overlap to the source edge. This structure enables enhanced vertical tunneling current by Si/SiGe hetero-junction (higher BTBT rate), with suppressing parasitic source edge component by Si/Si homo-junction (lower BTBT rate). Figure 11 shows Ioff characteristics of fabricated (a) P-type and (b) N-type hybrid Si and SiGe PP-TFETs and conventional Si or SiGe PP-TFETs. Much suppressed Ion with improved S.S. are successfully demonstrated with hybrid Si and SiGe PP-TFETs. It should be noted that gate leakage current (Ig) are also well suppressed with maintaining relatively thick EOT. This Ion level is 3 orders of magnitude lower than that of reported Si/SiGe hetero TFETs so far (Table 2).

Conclusion
Si/SiGe hetero PP-TFETs have been widely evaluated in consideration of appropriate SiGe configuration. It was confirmed that SiGe layer must be applied into source region in N-TFET and channel region in P-TFET respectively. Under this guideline, significantly large enhancement of Ion and Vth shift have been achieved both in P- and N-TFETs. Also, novel architecture with hybrid Si and SiGe PP-TFETs proposed and demonstrated extremely low Ion resulting in prominent Ion/Ioff ratio. This enables the realization of Si-based C-TFETs with current Si CMOS platform for ultra-low power applications.

Acknowledgement
This research was partially granted by JSPS through FIRST Program initiated by CSTP, Japan.
Fig. 1: Schematic diagrams of the structures for (a) lateral TFET and (b) PP-TFET. Significant Vdoff reduction and Imoff enhancement are observed in P-TFET with SiGe and in N-TFET with S-SiGe. However, opposite types of SiGe hetero samples show limited impact. This confirms appropriate configuration of SiGe application is necessary to boost ON-state current.

Fig. 2: Band diagram of ON-state of P- and N-type PP-TFETs. No visible dislocations are seen in all epi-ch layers. This suggests compressive strain is induced in SiGe layer. Note that very thin Si-cap layers on Ch-SiGe were consumed during gate stack and its pre-cleaning process.

Fig. 3: Ideal structure of complementary Si/SiGe hetero PP-TFET. SiGe application into channel region for P-TFET and source region for N-TFET are preferable to enhance ON-current.

Fig. 4: Process flow of Si/SiGe hetero PP-TFETs. SiGe-epi layers were formed as source or channel material. S/D and gate regions were defined by EB lithography. Source region was extended into the most of gate region. Drain region is kept away from gate edge by 200 nm to avoid ambipolar OFF-current.

Fig. 5: High resolution x-TEM images of fabricated PP-TFETs. No visible dislocations are seen in all epi-ch layers. This suggests compressive strain is induced in SiGe layer. Note that very thin Si-cap layers on Ch-SiGe were consumed during gate stack and its pre-cleaning process.

Fig. 6: Ioff/Ion characteristics of fabricated control sample of N-type Si/Ch-Si PP-TFETs with various Lg. It is confirmed that Lg proportionally increases with Lg. This indicates BTBT current in vertical direction is generated under the gate electrode.

Fig. 7: Ioff/Ion characteristics of fabricated PP-TFETs. (a) P-TFETs, (b) N-TFETs. Significant Vdoff reduction and Imoff enhancement are observed in P-TFET with Ch-SiGe and in N-TFET with S-SiGe. However, opposite types of SiGe hetero samples show limited impact. This confirms appropriate configuration of SiGe application is necessary to boost ON-state current.

Fig. 8: The dependence of Ioff/Ion characteristics on Ch-SiGe thickness in S-Si/Ch-SiGe PTFETs. Remarkable improvement in tunneling property is achieved with thicker Ch-SiGe thickness.

Fig. 9: Ioff/Ion characteristics of S-Si/Ch-SiGe in P-TFET with various Lg. It is seen that Lg increases with larger Lg in relatively high Lg level. Whereas that is not observed in lower level of Lg (Lg < 100). This indicates Imoff is dominated by not vertical tunneling current but parasitic source edge component.

Fig. 10: The concept of Si/SiGe hybrid PP-TFETs. Ch-SiGe or S-SiGe was removed by wet (SC1) patterning process so as to underlap to Si source edge. Only vertical tunneling current is enhanced by SiGe hetero junction while parasitic tunneling current at source edge in drain side is suppressed by Si/Si homo-junction.