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Mobility Model for Advanced SOI-MOSFETs Including Back-Gate Contributions

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Abstract

This paper reports a newly developed compact mobility model for very thin SOI and BOX layer MOSFETs. It is demonstrated that the universality of the low-field mobility is still preserved. However, the effective electric field is not only determined by the field induced at surface but modified by the potential distribution across the SOI layer. Measured *I-V* characteristics are well reproduced under a wide variety of bias conditions.

1. Introduction

The SOI (Silicon-on-Insulator) technology has been extended to very thin layers for both SOI and BOX in the SOTB-MOSFET generation, which enables a threshold voltage (V_{th}) control by the back-gate voltage [1]. The V_{th} control is exploited to realize reliable low voltage applications. The SOTB structure is close to the ultimate double-gate structure enabling higher circuit performance due to higher currents and additionally smaller subthreshold swing. This investigation aims at accurate compact modeling of these advantages, so that reliable circuit design becomes possible. The model must be applicable for any bias condition as well as structural variation. Our focus is the mobility model development. It is demonstrated that mobility universality is still applicable for the SOTB-device generation. However, the effective electric field is determined not only by the surface condition but by the total potential distribution across the SOI layer.

2. Characteristics of the SOTB-MOSFET

The SOTB-MOSFET structure and studied device dimensions are shown in Fig. 1. Measured device characteristics are shown in Fig. 2 as a function of V_{gs} for three V_{bg} values. It can be seen that subthreshold swing and current magnitude increase by positive biasing of V_{bg}.

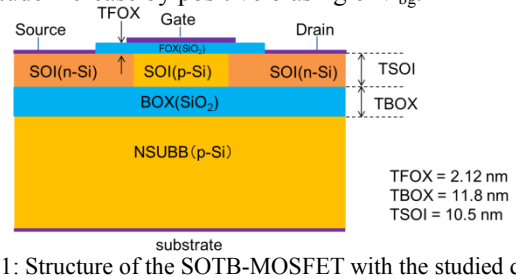

Figure 1: Structure of the SOTB-MOSFET with the studied device parameter values.

In addition to the impurity concentration in the SOI layer, that in the substrate determines the V_{bg} characteristics as well. Therefore, not only the device dimensions but also these impurity concentrations must be optimized.

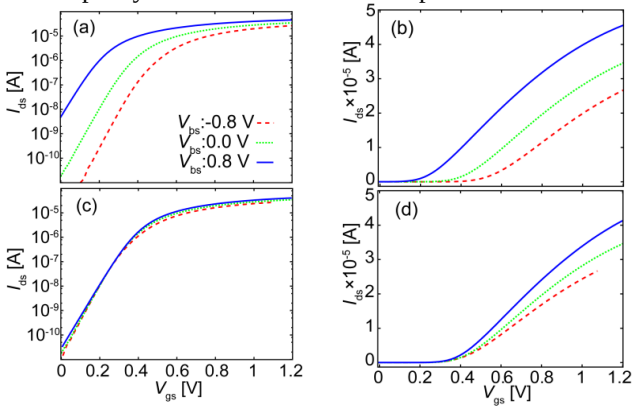

Figure 2: Measured SOTB-MOSFET I_d-V_g characteristics as a function of the gate voltage V_{gs}, (a) half logarithmic, (b) linear, (c) & (d) V_{th} shifted to the V_{bg}=0 value.

3. Analysis with 2D-device simulation

We apply 2D-device simulations for analyzing the important features of the SOTB-MOSFET. Fig. 3 shows 2D-simulations of the same characteristics as in Fig. 2 and verifies that measured features of Fig. 2 are reproduced.

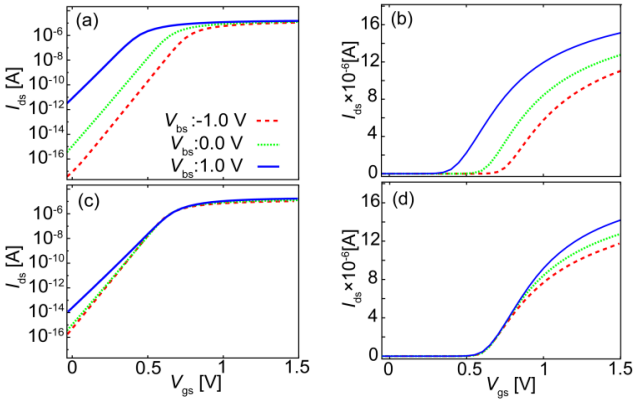

Figure 3: The same plot as in Fig.2 for 2D-device simulation results.

The I_{ds}-V_{gs} characteristics at V_{bg}=1V is analyzed in Fig. 4. It can be seen that the subthreshold current flows mostly at the back surface while the front-gate current dominates beyond V_{gs}=V_{th}. Fig. 5 shows the current distribution across the SOI layer for V_{gs}=0.5V and 1V. A clearly observed feature is that the current density is distributed within the whole SOI layer and not only located at surfaces even for V_{gs}=1V. This is exactly the important feature resulting from the thin SOI and BOX layers, which must be explicitly modeled.

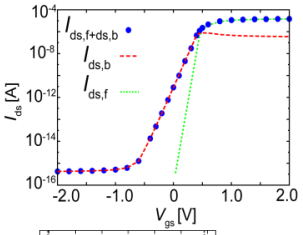

Figure 4: Simulated drain current I_{ds} separated into front surface part $I_{ds,f}$ and the back surface part $I_{ds,b}$.

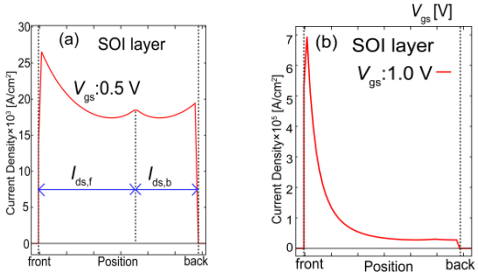

Figure 5: Simulated current distribution across the SOI layer, (a) for V_{gs}=0.5V and (b) for V_{gs}=1V.

4. Modeling of the SOTB-MOSFET

The potential distribution within the SOTB-MOSFET is a function of applied biases V_{gs} and V_{bg} as well as of the device parameters. To calculate the distribution accurately, the Poisson equation is solved iteratively together with boundary conditions for four potential values [2]

$$V_{gs} - V_{fb} - \phi_s = \frac{Q_i + Q_b + Q_{depSOI} + Q_{bulk}}{C_{FOX}} \quad (1)$$

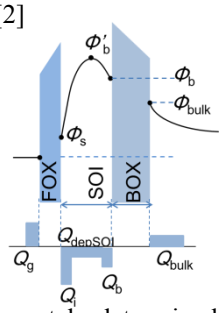

Figure 6: Schematic potential distribution across the SOI layer.

Once the potential distribution is accurately determined, all device characteristics are calculated as a function of the potential values. The drain current is calculated as

$$I = \frac{W}{L} \cdot \mu \cdot Q_i \cdot E_x \quad (2)$$

where Q_i is the mobile charge, μ is the mobility, and E_x is the electric field along the channel. The carrier mobility is determined by the field applied. The low field mobility is known to be described by the effective electric field E_{eff} vertical to the channel, preserving the universality verified for bulk MOSFETs [3] (see Fig. 7). The universality provides a simple way to analyze device characteristics. However, the electric field is not a simple function of the surface potential but determined by the whole potential distribution for the SOTB-MOSFET generation.

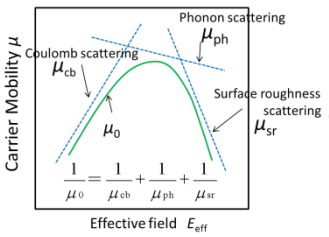

Figure 7: Mobility universality observed for the low field [3].

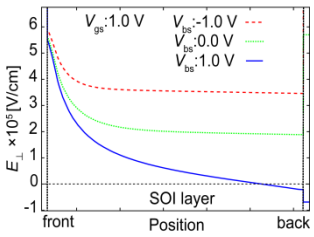

Figure 8: Simulated distribution of vertical electric field.

Therefore, accurate mobility modeling requires the derivation of an accurate analytical description of E_{eff}. Fig. 8 shows 2D-device simulation results of the E_{eff} distribution across the SOI layer for three V_{bg} values. It is verified that the effective electric field is not dominated by the surfaces and this feature must be correctly modeled.

The electric field at the back surface is determined by the potential difference between ϕ_b and ϕ_{bulk} written together with the Gauss law as

$$E_{eff,b} = \frac{\varepsilon_{BOX}}{\varepsilon_{SOI}} \cdot -\frac{\phi_{bulk} - \phi_b}{T_{BOX}} \quad (3)$$

Since the front surface potential is determined under the influence of the back-gate potential, $E_{eff,F}$ is written as the sum of both fields as

$$E_{eff,F} = E_{eff,f} + E_{eff,b} \; ; E_{eff,f} = \frac{\gamma \cdot Q_{depSOI} + \eta \cdot Q_i}{\varepsilon_{Si}} \quad (4)$$

where the front electric field is calculated by the potential values of ϕ_s and ϕ_b' (see Fig. 6). Fig. 9 summarizes the comparison of calculated E_{eff} values with those of 2D-device simulations, showing good agreement.

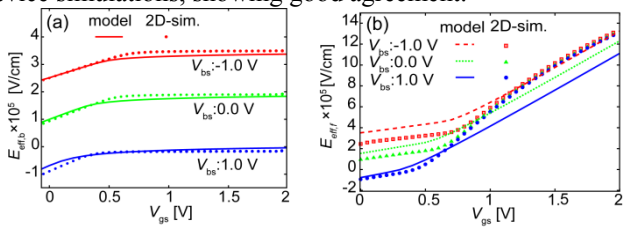

Figure 9: Comparison of calculated effective electric field with 2D-device simulation results, (a) at the back surface and (b) at the front surface.

The high field mobility is written as the usual function of the lateral electric field. By using of the developed model I_{ds}-V_{gs} characteristics have been fitted to measurements. Examples for the accurately agreeing results are shown in Fig. 10.

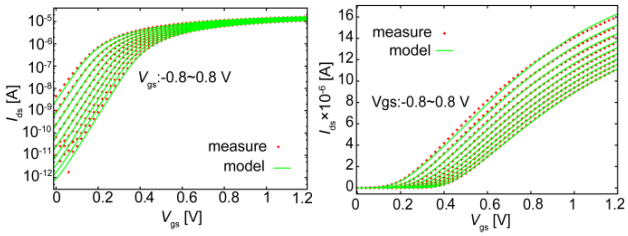

Figure 10: Comparison of calculated I_{ds}-V_{gs} characteristics by the developed model with measurements.

5. Conclusions

The potential distribution in MOSFETs with thin SOI and BOX layers is very sensitive to device parameters as well as bias conditions. By solving the Poisson equation for the complete SOTB-structure an accurate compact mobility model could be developed for both the front and the back surface currents of the thin SOI layer.

References

[1] R. Tsuchiya et al., IEDM Tech Dig., 631, 2004.
[2] M Miura-Mattausch et al., IEEE TED, vol. 61, 255, 2014.
[3] A. G. Savinis et al., IEDM tech Dig., 18, 1979; S. Takagi et al., IEDM tech Dig., 398, 1988.