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On the Importance of Electron-electron Scattering for Hot-carrier Degradation

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Abstract

Using our physics based model for hot-carrier degradation (HCD) we analyze the effect of electron-electron scattering (EES) on HCD in devices with different channel lengths. We show that – in contrast to recent suggestions – EES does play a crucial role in ultra-scaled MOSFETs and can be important also in long transistors with the lengths as long as 300nm.

1. Introduction

The rapid miniaturization of MOSFETs has led to operating voltages scaled below 1V. As a result, hot-carrier degradation has evolved from a mode where the damage is produced primarily by solitary hot carriers to a regime in which a substantial contribution is made by colder carriers [1,2]. As a consequence, HCD appears to be highly sensitive to the way carriers are distributed over energy because high and low energetical particles can trigger different bond dissociation mechanisms. The former information is contained in the carrier energy distribution function (DF). Its shape is formed by scattering mechanisms which need to be considered self-consistently with bond-breakage processes [3]. One of these mechanisms which plays a crucial role in ultra-scaled devices is EES which populates the high-energy tails of the DF far beyond energies available from the electric field [4]. Moreover, Rauch *et al.*, have reported that this mechanism is responsible for severe HCD reinforcement in transistors from the 180nm node and beyond [5]. Quite to the contrary, the group of Bravaix suggested that in their devices the role of EES is substantially overestimated [6]. Using our recently developed physics-based HCD model [3] we investigate the importance of EES in the context of HCD in short- and long-channel transistors.

2. The Modeling Framework.

The model is capable of representing HCD in three different MOSFETs of identical architecture (with a 2.5nm SiON film) but different gate lengths (65, 100, and 150nm) stressed at different combinations of V_{ds} and V_{gs} for a period of ~8ks (Fig. 1) using a unique set of model parameters. Our approach covers and links three main aspects of HCD [2,3]: carrier transport, microscopic mechanisms of defect generation, and modeling of the degraded devices, Fig. 2. The model is implemented into the deterministic Boltzmann transport equation solver ViennaSHE. The scattering mechanisms and Si-H bond-breakage processes are considered self-consistently. A bond rupture event can be triggered by a single hot carrier, which excites one of the bonding electrons to an antibonding state (AB-mechanism). A series of colder carriers can induce bond-breakage by the multiple vibrational excitation (MVE-process) of the bond. Another important ingredient of HCD, i.e. the dispersion of the bond-breakage energy and its reduction due to the dipole-field interaction, are also incorporated into the model. ViennaSHE evaluates the carrier DF for a particular device topology and stress condition. As the DF is very sensitive to the doping profiles, the MOSFET structures are obtained using the Sentaurus Process simulator calibrated and coupled to ViennaSHE to represent characteristics of the fresh devices. In order to analyze the effect of EES on HCD in transistors with different channel lengths we also simulated structures of devices with gate lengths of 44, 200, and 300nm.

3. Results and Discussions

Fig. 1. summarizes the experimental change of the linear drain current ΔI_{dlin} as a function of time plotted vs. simulated ones. The $\Delta I_{dlin}(t)$ curves obtained neglecting EES fail to represent HCD in 65 and 100nm device for both combinations of voltages. Note that the discrepancy between $\Delta I_{dlin}(t)$ simulated with and without EES increases with $\{V_{ds},V_{gs}\}$. In the 44nm transistor, the effect of EES is pronounced already at such low voltages as V_{ds}= 1.2, V_{gs}=0.8V, Fig. 3. As for the opposite case of long-channel devices, Fig. 4 depicts a series of DFs calculated near the drain end of the gate with and without EES. Electron-electron scattering populates the high energetical fraction of the carrier ensemble. This is visible in Fig. 4 as an offset of the hump in the high-energy DF tail. Note that at lower $\{V_{ds},V_{gs}\}$ these humps appear much later and corresponding hotter carriers do not significantly contribute to HCD. This is in good agreement with Fig. 5 where the ratios between ΔI_{dlin} obtained disregarding one of the model ingredients and those simulated using the full model are plotted. One can see that if transistors with the gate lengths of 200 and 300nm are stressed at V_{ds}=2.4, V_{gs}=1.4V, EES still plays an important role, while at lower voltages its effect is much weaker. Therefore, these findings show that rather than the transistor channel length alone, the combination of device dimensions and the stress voltages controls whether EES contributes to hot-carrier damage or not.

3. Conclusions

Using our physics-based HCD model we have demonstrated that EES is important for hot-carrier degradation. We conclude that rather than the channel length alone, the combination of the device architecture and applied voltages

determines the role of EES. Thus, even in long MOSFETs with a gate length of 300nm, EES can play a significant role at voltages of V_{ds}=2.8, V_{gs}=1.4V and higher.

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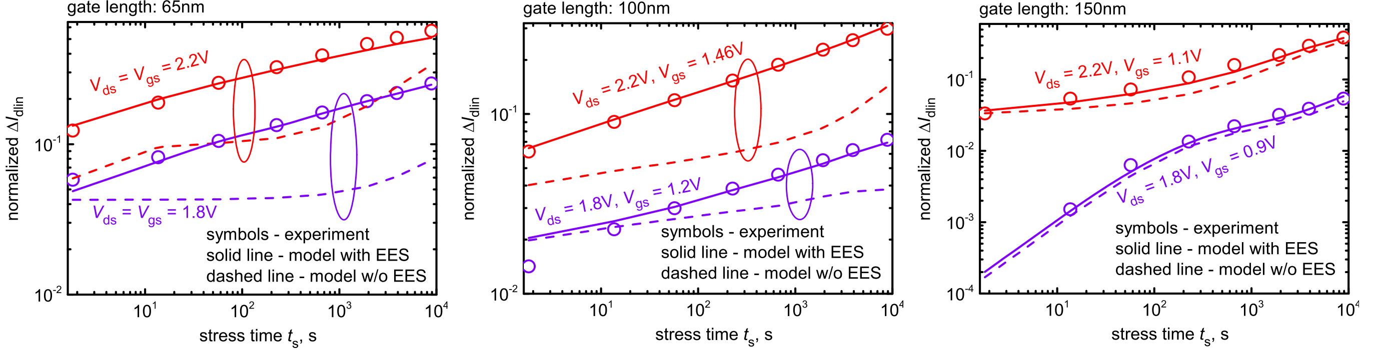

Fig. 1. The normalized (i.e. divided by the drain current of the fresh device) linear drain current change $\Delta I_{dlin}(t)$ measured in three different MOSFETs with the gate lengths of 65, 100, and 150nm. The devices were stressed at their corresponding HCD worst-case conditions at V_{ds}=1.8 and 2.2V. For comparison, we also plot $\Delta I_{dlin}(t)$ obtained without EES. In 65 and 100nm transistors $\Delta I_{dlin}(t)$ is substantially underestimated if EES is ignored.

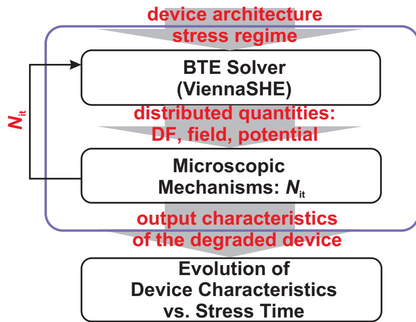

Fig. 2. Our HCD model contains the carrier transport kernel, the module which describes the trap generation kinetics, and the degraded device characteristic simulator.

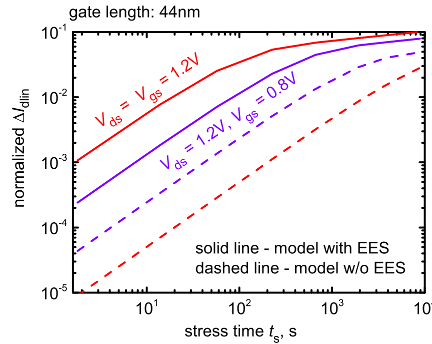

Fig. 3. The $\Delta I_{dlin}(t)$ curves modeled in the MOSFET with the gate length of 44nm for V_{ds}=1.2V, V_{gs}=0.8V and V_{ds}=V_{gs}=1.2V considering and ignoring EES.

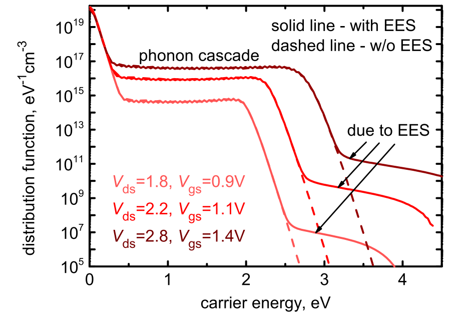

Fig. 4. The series of the DFs obtained for the 300nm MOSFET and three different combinations of V_{ds} and V_{gs}. The humps pronounced at high energies are due to EES.

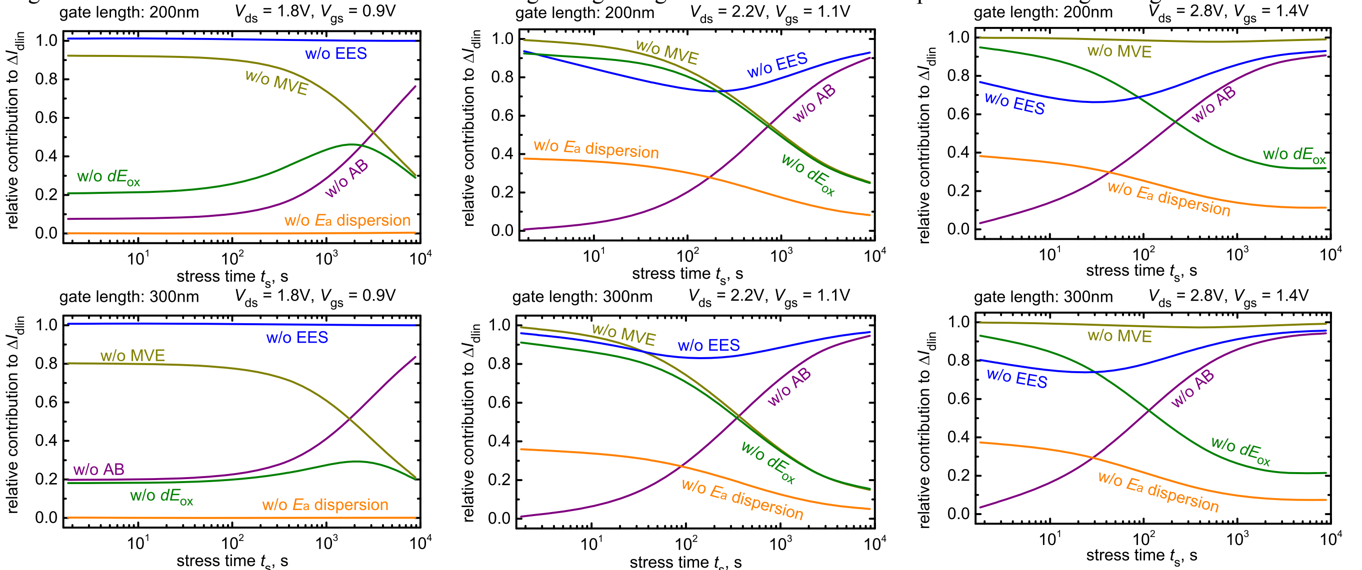

Fig. 5. The ratio between ΔI_{dlin} obtained disregarding one of the model components and that calculated with the full model plotted for the devices with the gate lengths of 200 and 300nm. The relative EES contribution becomes more pronounced at higher $\{V_{ds},V_{gs}\}$ and appears to be weaker in longer devices. However, even in the 300nm MOSFET this mechanism can provide a substantial contribution to HCD.