

Drive Current Performance of Inversion Mode Ge CMOS Transistors

Xiao Gong* and Yee-Chia Yeo.

Department of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore 117576.

*Phone: +65-6516-1589, Fax: +65-6779-1103, Email: elegong@nus.edu.sg

I. Introduction

Germanium (Ge) is a promising alternative channel material for future complementary metal-oxide-semiconductor (CMOS) technology due to its high electron and hole mobilities. In the past decade, significant effort has been made in the research community to bring this material as a possible high-mobility replacement for silicon which has been the dominant channel material in CMOS technology for almost 50 years [1]-[25]. To exploit the full potential of the high mobility property of Ge, one of the key issues is the formation of thermodynamically stable Ge/gate dielectrics interface with low interface trap density (D_{it}), small equivalent oxide thickness (EOT), and low gate leakage current.

In this paper, drive current performance benchmarking for inversion mode Ge CMOS is performed. This is done with a specific focus on a recently reported passivation technique using an ultra-thin InAlP layer for both n-channel field-effect-transistors (nFETs) and p-channel FETs (pFETs). We will also discuss the recent progress in the gate stack formation on Ge using various surface passivation techniques, and the benchmarking of electrical characteristics for Ge nFETs and pFETs.

II. InAlP as a Common Passivation Technique for Ge nFETs and pFETs

Fig. 1 shows a recently reported concept of forming a high-quality, epitaxial, single crystalline, and potentially defect-free interfacial layer on the Ge channel and beneath the gate dielectric. An excellent material candidate is $\text{In}_{0.48}\text{Al}_{0.52}\text{P}$, which is lattice-matched to Ge and has a relatively large bandgap of 2.36 eV. InAlP can be epitaxially grown on Ge by MOCVD prior to high- k dielectric deposition. Using X-ray Photoelectron Spectroscopy, it was found that InAlP has a conduction band offset (ΔE_C) and valence band offset (ΔE_V) of 0.84 and 0.86 eV, respectively, with respect to Ge [Fig. 2 (a)] [2]. These band offsets between InAlP and Ge are large enough to confine the electrons in Ge channel in nFETs and holes in the Ge channel in pFETs, as illustrated in the energy band diagrams of pFETs and nFETs at strong inversion regime in Fig. 2 (b). The InAlP layer separates the carriers from the interface traps at the high- k /InAlP interface, leading to reduced carrier scattering and enhanced carrier mobility.

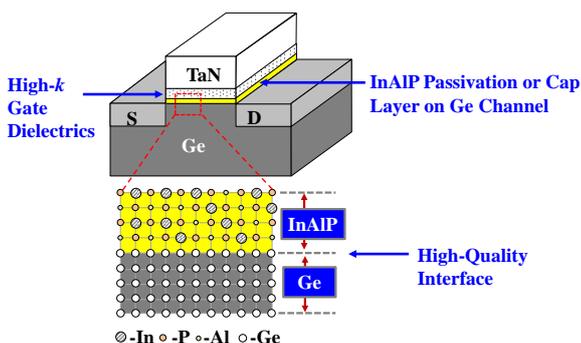


Fig. 1. 3-D schematic showing an InAlP layer sandwiched between the high- k gate dielectrics and Ge channel. The single crystalline InAlP layer can be epitaxially grown on the lattice-matched Ge surface prior to the high- k dielectric and metal gate deposition.

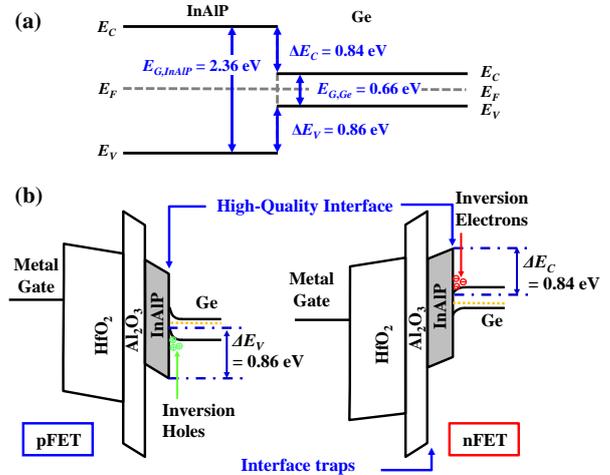


Fig. 2. (a) Energy band diagram showing that the InAlP/Ge interface has a ΔE_C of ~ 0.84 eV and a valence band offset ΔE_V of ~ 0.86 eV. (b) Band diagrams of an InAlP-capped Ge pFET and nFET at strong inversion regime. Holes and electrons are confined in the Ge layer by the InAlP cap due to the large band offsets.

III. Benchmarking of Germanium nFETs

Fig. 3 (a) and (b) plot the $I_{DS}-V_{GS}$ curves at V_{DS} of 0.05 and 1 V, respectively, of InAlP-capped Ge (100) nFETs and other planar Ge (100) nFETs by various passivation techniques reported in literature. For both high and low V_{DS} , the InAlP-capped Ge nFETs exhibit subthreshold swing S of less than 110 mV/decade and On-state current to Off-state current

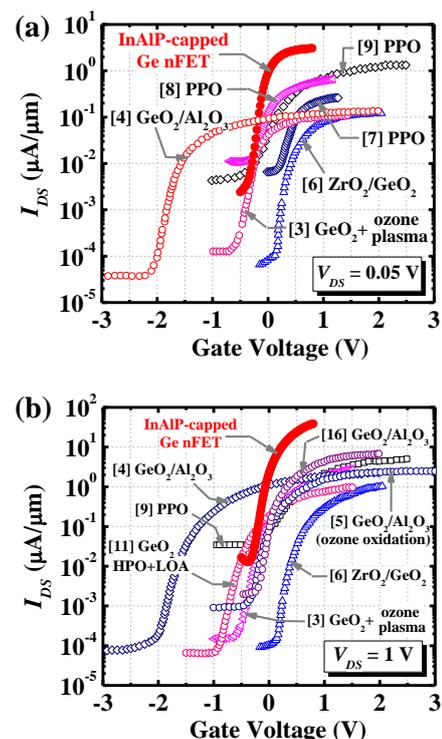


Fig. 3. $I_{DS}-V_{GS}$ curves at (a) V_{DS} of 0.05 and (b) 1 V of InAlP-capped Ge (100) nFETs and other planar Ge (100) nFETs by various passivation techniques reported in literature. High I_{ON} , high I_{ON}/I_{OFF} ratio, and excellent S were achieved for InAlP-capped Ge nFETs.

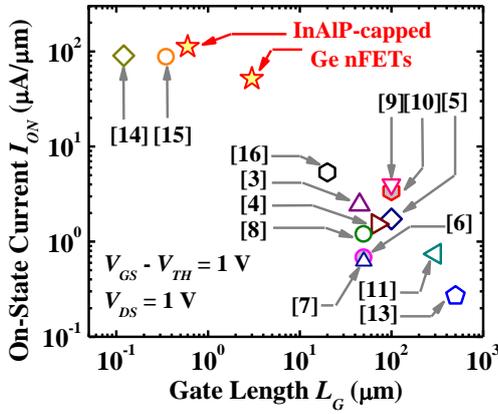


Fig. 4. Record high drive current of 112 $\mu\text{A}/\mu\text{m}$ was achieved for enhancement mode Ge nFETs at $V_{GS}-V_{TH}$ of 1 V and V_{DS} of 1 V though the L_G is not the shortest.

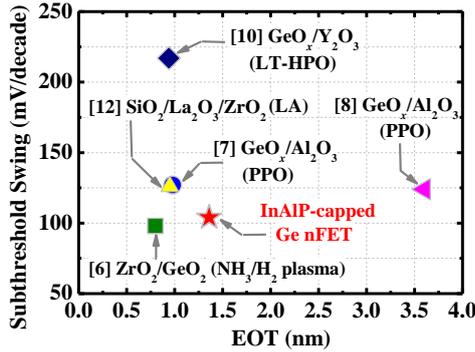


Fig. 5. S values as a function of EOT for long channel planar Ge nFETs with different surface passivation techniques. InAlP passivation leads to the realization of Ge nFETs with S comparable to the best reported values.

ratio (I_{ON}/I_{OFF}) close to 4 orders. To have a better comparison, Fig. 4 plots I_{ON} as a function of gate length L_G for Ge nFETs. Note that the data points in Ref. 14 and Ref. 15 are from FinFETs where L_G values are much smaller than others. For the InAlP-capped Ge nFET with a L_G of 3 μm , I_{ON} is ~ 50 $\mu\text{A}/\mu\text{m}$ at $V_{GS}-V_{TH}$ of 1 V and V_{DS} of 1 V. At L_G of 600 nm, the InAlP-capped Ge nFET achieves the record high I_{ON} of 112 $\mu\text{A}/\mu\text{m}$ for Ge inversion mode nFETs although L_G is not the shortest. In addition to the high I_{ON} , InAlP-capped Ge nFETs also exhibit S comparable to the best reported values, as indicated Fig. 5 where S values are plotted as a function of the EOT of long channel planar Ge nFETs. With further scaling of EOT, much higher I_{ON} and better S are expected. The scaling of EOT can be realized by reducing the InAlP thickness during the epitaxial growth and by reducing the thickness of high- k gate dielectrics.

Fig. 6 shows peak electron mobility μ_{eff} values for (100)-oriented Ge nFETs using various passivation techniques. The InAlP cap helps to achieve the highest reported peak μ_{eff} of ~ 1060 $\text{cm}^2/\text{V}\cdot\text{s}$ for (100)-oriented Ge nFETs. Further process optimization is needed to improve μ_{eff} in the high N_{inv} regime.

IV. Benchmarking of Germanium pFETs

From cost-effective point of view, a common passivation technique is preferred for both Ge nFETs and pFETs. As discussed in Section II, in addition to a large ΔE_C of 0.84 eV between InAlP and Ge, there is also a ΔE_V of 0.86 eV between

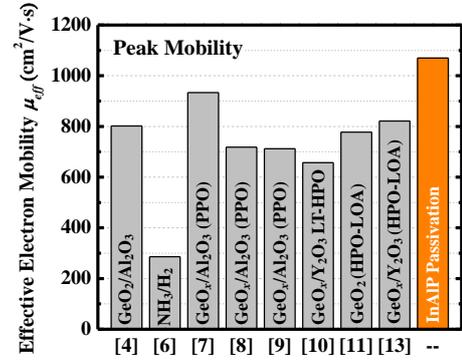


Fig. 6. Benchmark of peak electron mobility μ_{eff} for (100)-oriented Ge nFETs using various passivation techniques in literature. InAlP-capped Ge nFETs show peak μ_{eff} of ~ 1060 $\text{cm}^2/\text{V}\cdot\text{s}$ which is the highest reported value for Ge nFETs fabricated on Ge (100) substrates.

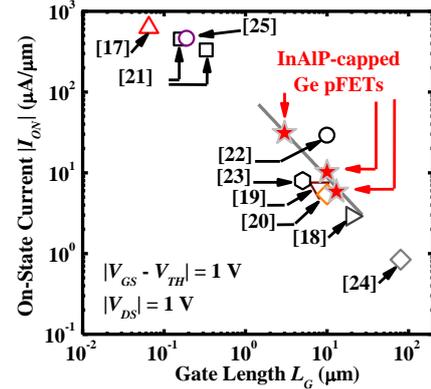


Fig. 7. Benchmarking of I_{ON} at $|V_{GS}-V_{TH}| = 1$ V and $|V_{DS}| = 1$ V of the Ge pFETs with the InAlP cap with other I_{ON} estimated at the similar bias conditions from the literature. Very high I_{ON} was achieved for the InAlP-capped Ge pFETs.

the two. This indicates that InAlP can also be a good passivation layer for Ge pFETs. I_{ON} of the InAlP-capped Ge pFETs are compared with those of other Ge pFETs using different passivation techniques in literature (Fig. 7). I_{ON} was extracted at $|V_{GS}-V_{TH}|$ of 1 V and $|V_{DS}|$ of 1 V. The InAlP-capped Ge pFETs show high I_{ON} at relatively large L_G .

V. Conclusion

We compared the electrical characteristics of InAlP-capped Ge nFETs and pFETs with various surface passivation techniques. The benchmarking shows that InAlP is a promising passivation technique for the gate stack formation for both nFETs and pFETs in future high performance and low power logic applications.

References

- [1] B. Liu et al., IEDM 2013, p. 756
- [2] M. Owen et al., APL 103, 031604, 2013
- [3] Y. C. Fu et al., IEDM 2010, p. 432
- [4] K. Morii et al., IEDM 2009, p. 681
- [5] D. Kuzum et al., IEDM 2009, p. 453
- [6] C. M. Lin et al., IEDM 2012, p. 509
- [7] R. Zhang et al., IEDM 2011, p. 642
- [8] R. Zhang et al., IEDM 2012, p. 371
- [9] R. Zhang et al., VLSI 2013, p. T26
- [10] C. H. Lee et al., VLSI 2013, p. T28
- [11] C. H. Lee et al., IEDM 2009, p. 457
- [12] W. Chen et al., IEDM 2010, p. 420
- [13] C. H. Lee et al., IEDM 2010, p. 416
- [14] C. T. Chung et al., IEDM 2012, p. 383
- [15] S. H. Hsu et al., IEDM 2012, p. 525
- [16] G. Thareja et al., IEDM 2010, p. 245
- [17] J. Mitard et al., IEDM 2008, p. 873
- [18] N. Wu, et al., EDL 25, p. 631, 2004
- [19] S. Zhu et al., EDL 26, p. 81, 2005
- [20] A. Ritenour et al., IEDM 2003, p.18.2.1
- [21] B. Liu, et al., EDL 33, p. 1336, 2012
- [22] R. Xie et al., IEDM 2008, p. 393
- [23] R. Zhang et al., VLSI 2012, p. 161
- [24] Y. Kamata et al., VLSI 2009, p. 78
- [25] P. Zimmerman et al., IEDM 2006, p.655