Strained Si₀.₁Ge₀.₉ on Strained-Si-on-Insulator (sSOI) pMOSFETs for Low-Power sSOI based CMOS

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Abstract

We demonstrate a high hole mobility (µ‌ₚₑₜ = 475 cm²/Vs at Nₜ = 5x10¹⁲ cm⁻²) in strained-Si₀.₁Ge₀.₉ on sSOI pMOSFET of which channel was directly grown on a strained-Si on insulator (sSOI) substrate for the first time. The best subthreshold slope value (Sₛₛ = 78 mV/dec) among strained-Ge or Ge-rich SiGe channel pMOSFETs was obtained. The use of an alloy channel rather than pure Ge one is a key to realize such excellent mobility and Sₛₛ values simultaneously because of the suppression of dislocation introduction and hole generation in the channel in spite of the large misfit strain.

Introduction

High mobility channel materials are widely explored to replace Si in MOSFET devices to suppress the power consumption by lowering substrateopping voltages (Vₛₛ) and improving circuit performance. Strained-Ge[1-6] and strained-SiGe[7-10] is promising option for p-channel FETs due to its significantly high hole-mobility and compatibility with Si-CMOS process. On the other hand, strained SiGe devices such as Strained-Si-on-Insulator (sSOI)[11] extensively investigated as a 22nm node and beyond[7-10]. Excellent high performance is achieved for low-power application owing to better short channel control. However, several key challenges remain to achieve high-performance. In the embedded stressor is less effective to these devices[8]. Although, introducing of strained-Si on insulator (sSOI) channel is a promising solution as a performance booster for pFET, tensile strain of sSOI channel degrades hole-mobility in pFET. To improve the pFET performance, strained-SiGe channel which formed by local Ge condensation was demonstrated[7-10]. However, Ge content in SiGe channel is less than 35% and much higher content is required for high mobility. Here, direct epitaxial growth of Ge on sSOI on the pFET regions is a promising and simpler way to obtain higher mobility p-channels. In general, however, it is difficult to eliminate dislocation introduction in such high misfit strain system. Actually, SiGe-shell nanowire pMOSFET have been demonstrated by Hashemi et. al, with CMOS compatible top-down approach using selective epitaxial growth of pure-Ge on SOI fin structure[11]. But its hole mobility was severely deteriorated to less than ~80 cm²/Vs caused by dislocation introduction into Ge shell. In this paper, we demonstrate that a Ge-rich SiGe alloy channel on sSOI is more beneficial to avoid dislocation introduction and to realize high performance. By combining of Ge and SiGe, Semipseudomorphically strained Ge-rich SiGe alloy (Si₀.₉Ge₀.₁) channel MOSFETs on sSOI substrate having a TaN / Si passivation / H₂O gate stacks were fabricated and a high effective hole mobility (µₑₜ = 475 cm²/Vs at Nₜ = 5x10¹² cm⁻²) was obtained in 5.5x10⁻¹⁰ cm²/Vs dependence on the channel thickness, 250 nm. The Sₛₛ value (78 mV/dec) of 5nm-thick Ge channel was achieved simultaneously.

Device fabrication

Figure 1 shows a concept of proposed CMOS, featuring sSOI channel for nFET and strained (Si/Ge) channel on sSOI for pFET. This architecture can enjoy the high mobility channels by simple process steps compared with local Ge condensation. Key fabrication steps of strained-(Si/Ge) channel on sSOI MOSFETs are summarized in Fig. 2. Firstly, strained-Si channel was formed by mesa etching of sSOI (~1% biaxial tensile strain) substrates. Here, anisotropic strain relaxation of strained-Si mesa induced uniaxial stress along the channel direction to narrow fins. Then, hydrogen annealing at 850°C was carried out to improve channel surface roughness and shrinkage of fin width. After that, strained-(Si/Ge) channel and 1-nm thick Si passivation were grown by RPCVD at 380°C only for pFETs. A 4-nm H₂O layer was then grown by using an atomic layer deposition system. Figure 3 shows a TEM of the narrowest channel with a core-Si width (Wₙₐ₉) of 28nm. It is clearly seen that smooth and circular shape of strained-Si core due to the effect of hydrogen annealing. Moreover, sidewalls of SiGe channel was mainly formed on the (111) facets. Figure 4 shows the comparison of xTEM between pure-Ge on sSOI and Si₀.₉Ge₀.₁ on sSOI. In pure-Ge on sSOI, dislocation which formed by strain relaxation was observed. On the other hands, dislocation formation is improved in Si₀.₉Ge₀.₁ on sSOI. The obtained dislocation density is measured in the SiGe alloy channel by analyzing TEM lattice fringe. The Wₙ₉ dependence of measured Raman peak shift, Δν₉ is shown in Fig.5(a). Extremely high (over -2.7x) compressive strain, which is almost identical with the misfit strain between Si₀.₉Ge₀.₁ on sSOI core (εₓₓ = 2~6 %) and comparison of the remaining strain in channel direction, εₓₓ, in pure-Ge and Si₀.₉Ge₀.₁ channels are shown in Fig.5(b). The Si₀.₉Ge₀.₁ channel has larger εₓₓ than that for pure-Ge because of suppression of dislocation formation by alloy effect[12].

Hole-mobility characterization

Hole mobility was extracted by a split CV method for long-channel and multi-wire devices. Nₜ is the average surface carrier density defined by Nₜ = N₋₁ (Wₓₓ + 2 Wₙ₉), where N₋₁ is the liner inversion carrier density obtained from CV measurement. Wₓₓ and Wₙ₉ represent the wire width on top surface and length of faceted edges, respectively as shown in Fig. 4(a). Figure 6 shows the comparison of µₑₜ dependence of peak mobility, µₑₜ for “thick” (εₓₓ = 4~8 nm) and “thin” (εₓₓ = 2~6 nm) anisotropically strained Si₀.₉Ge₀.₁ on sSOI pMOSFETs with different core width, Wₙ₉. The hole mobility was decreased by shrinking Wₙ₉, Figure 7 shows the comparison of Wₙ₉ dependence of peak mobility between strained Si₀.₉Ge₀.₁ on sSOI and pure Ge on sSOI were used for comparative evaluation. Thanks to high compressive strain along the channel and less defective condition at the sSOI-SiGe heterointerface, the Si₀.₉Ge₀.₁ on sSOI shows the highest mobility of 597 cm²/Vs at Nₜ = 6.0x10¹⁰ cm⁻² even though the mobility of pure Ge on sSOI was less than 360 cm²/Vs. This result suggests that the advantage of Si₀.₉Ge₀.₁ in terms of the suppression of dislocation because of high Ge content. The Sₛₛ value was also improved as shown in Fig. 7. Figure 8 shows the effective hole mobility, µₑₜ of anisotropically strained Si₀.₉Ge₀.₁ on sSOI MOSFETs with different core width, Wₙ₉. The hole mobility was decreased by shrinking Wₙ₉, Figure 9 shows the comparison of Wₙ₉ dependence of peak mobility between strained Si₀.₉Ge₀.₁ on sSOI and Si₀.₉Ge₀.₁ on sSOI pMOSFETs. At wide Wₙ₉ region, mobility of Si₀.₉Ge₀.₁ on sSOI was increased with decreasing Wₙ₉ even though the mobility of strained Si₀.₉Ge₀.₁ on SOI was almost unchanged. This mobility improvement can be explainable by the effect of anisotropic strain applied in Si₀.₉Ge₀.₁ on sSOI. On the other hands, at narrow Wₙ₉ region, mobility was severely degraded at both devices. This effect might be due to the increased contribution of (111) sidewalls. To understand this strain and sidewall effect, “thin” strained Si₀.₉Ge₀.₁ on sSOI core pMOSFETs was evaluated. Figure 10 shows the comparison of Wₙ₉ dependence of peak mobility, µₑₜ for “thick” (εₓₓ = 4~8 nm) and “thin” (εₓₓ = 2~6 nm) anisotropically strained Si₀.₉Ge₀.₁ on sSOI pMOSFETs. The mobility enhancement by “thin” strained Si₀.₉Ge₀.₁ channel was also achieved. And almost same mobility improvement was observed on the p-channel MOSFETs. Figure 11 shows the comparison of Wₙ₉ dependence of threshold voltage shift, ΔVₛₛ between “thick” and “thin” strained Si₀.₉Ge₀.₁ on sSOI. The Vₛₛ of “thick” strained Si₀.₉Ge₀.₁ was negatively shifted by decreasing Wₙ₉. The negative Vₛₛ shift is attributed to the valence band energy modulation by changing the strain from biaxial to uniaxial. On the other hands, the Vₛₛ of “thick” strained Si₀.₉Ge₀.₁ was positively shifted by decreasing Wₙ₉. Moreover, threshold voltage shift, ΔVₛₛ of “thick” strained Si₀.₉Ge₀.₁ was also positively increased by decreasing Wₙ₉ even though that for “thick” strained Si₀.₉Ge₀.₁ was improved (Fig.12). These results suggest that the Dₛₛ at (111) sidewalls and/or hole generation in the channel deteriorate the Sₛₛ values. And it might be suppressed by thinning the strained Si₀.₉Ge₀.₁ channel. In order to benchmark the performance for low-power operation, Fig. 13 shows a metrics of hole mobility enhancement factor against Si at Nₜ = 5x10¹² cm⁻² versus substrate slope, Sₛₛ. The obtained combination of hole mobility enhancement factor of 7.7 against that of a Si counterpart and Sₛₛ. value of 78mV/dec. exhibits a potential to reduce the |Vₛₛ| lower than 0.5V with keeping a comparable intrinsic gate delay.

Conclusions

Anisotropically strained Si₀.₉Ge₀.₁ on sSOI pMOSFETs with high hole mobility and excellent Sₛₛ values were demonstrated. The alloy channel was shown to be beneficial to prevent the lattice relaxation in spite of the large Ge content. The obtained combination of hole mobility enhancement factor of 7.7 against that of a Si counterpart and Sₛₛ value of 78mV/dec. exhibits a potential to reduce the |Vₛₛ| lower than 0.5V with keeping a comparable intrinsic gate delay. The result indicates that strained Ge-rich SiGe on sSOI pMOSFETs are promising for low-power sSOI-CMOS LSIs.

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Fig. 2 Fabrication process of strained-Si core/strained-(Si)Ge shell MOSFETs with Si passivation/HfO2 gate stack. 

Fig. 3 Cross-sectional TEM image of strained Si0.1Ge0.9-shell on sSi core with the narrowest core-Si width of 28nm.

Fig. 4 Cross-sectional TEM images of (a) Ge on sSOI and (b) Si0.1Ge0.9 on sSOI after full processing. Dislocation formation in shell channel is effectively suppressed by Si incorporation.

Fig. 5 (a) Measured Raman peak shift, $\Delta \omega$ of Ge-Ge peak and (b) Comparison of remaining strain in channel direction, $\epsilon_{xx}$ in pure-Ge and Si0.1Ge0.9 channels $\epsilon_{xx}$ at biaxial strained wide $W_{\text{core}}$.

Fig. 6 Comparison of effective hole mobility, $\mu_{\text{eff}}$ of anisotropically strained (Si)Ge pMOSFETs ($W_{\text{core}} = 145$nm) with different cores.

Fig. 7 Comparison of $I_D-\mathcal{V}_G$ characteristics of strained Si0.1Ge0.9 on sSOI and pure Ge on sSOI pMOSFETs.

Fig. 8 Comparison of $W_{\text{core}}$ dependence of peak mobility, $\mu_{\text{peak}}$ for strained Si0.1Ge0.9 on sSOI and strained Si0.1Ge0.9 on SOI pMOSFETs.

Fig. 9 Comparison of $W_{\text{core}}$ dependence of peak mobility, $\mu_{\text{peak}}$ for “Thick” ($W_{\text{core}} = 4-8$ nm)” and “Thin” ($W_{\text{core}} = 2-6$ nm)” anisotropically strained Si0.1Ge0.9 on sSOI pMOSFETs.

Fig. 11 Core width, $W_{\text{core}}$ dependence of linear threshold voltage shift, $\Delta \mathcal{V}_{\text{TH}}$.

Fig. 13 Benchmark of hole mobility enhancement factor with respect to MG/HK Si counterpart [13] vs S.S. Lines show required mobility enhancement at each $|V_{\text{th}}|$. Larger mobility enhancement with lower S.S. can reduce $|V_{\text{th}}|$ under the constant CVII.