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Strained $Si_{0.1}Ge_{0.9}$ on Strained-Si-on-Insulator (sSOI) pMOSFETs for Low-Power sSOI based CMOS

Keiji Ikeda[*)], Yoshihiko Moriyama, Toshifumi Irisawa, Mizuki Ono, Yuuichi Kamimuta, Minoru Oda, Tomonori Miyaki, Etsuo Kurosawa and Tsutomu Tezuka
Collaborative Research Team Green Nanoelectronics Center (GNC),
National Institute of Advanced Industrial Science and Technology (AIST), Onogawa 16-1, Tsukuba, Ibaraki 305-8569, Japan.
[*)] *Present address: Toshiba Corporation* E-mail : *keiji.ikeda@toshiba.co.jp*

Abstract

We demonstrate a high hole mobility (μ_{eff} = 475 cm^2/Vs at N_s = 5.0x10^{12}cm^{-2}) of an anisotropically strained $Si_{0.1}Ge_{0.9}$ pMOSFET of which channel was directly grown on a strained-Si on insulator (sSOI) substrate for the first time. The best subthreshold slope value (*S.S.* = 78 mV/dec.) among strained-Ge or Ge-rich SiGe channel pMOSFETs was obtained. The use of an alloy channel rather than pure Ge one is a key to realize such excellent mobility and *S.S.* values simultaneously because of the suppression of dislocation introduction and hole generation in the channel in spite of the large misfit strain.

Introduction

High mobility channel materials are widely explored to replace Si in MOSFET devices to suppress the power consumption by lowering supply voltages, V_{dd}, without degrading circuit performance. strained-Ge[1-6] and strained-SiGe[7-10] is promising option for p-channel FETs due to its significantly high hole-mobility and compatibility with Si-CMOS process. On the other hands, FD-SOI devices such as ETSOI and UTBB have been extensively investigated as a 22nm node and beyond[7-10]. Excellent performance is achieved for low-power application owing to better short channel control. However, several key challenge is remain to achieve high-performance because of the embedded stressor is less effective to these devices[8]. Although, introducing of strained-Si on insulator (sSOI) channel is a promising solution as a performance booster for nFET, tensile strain of sSOI channel degrades hole-mobility in pFET. To improve the pFET performance, strained-SiGe channel which formed by local Ge condensation have been demonstrated[7-10]. However, Ge content in SiGe channel is less than 35% and much higher Ge content is required for further mobility enhancement. Here, direct epitaxial growth of Ge on sSOI on the pFETs regions is a promising and simpler way to obtain higher mobility p-channels. In general, however, it is difficult to eliminate dislocation introduction in such high misfit-strain system. Actually, Si-core/Ge-shell nanowire pMOSFET have been demonstrated by Hashemi *et. al.* with CMOS compatible top-down approach using selective epitaxial growth of pure-Ge on SOI fin structure[11]. But its hole mobility was severely deteriorated to less than ~80 cm^2/Vs caused by dislocation introduction into Ge shell. In this paper, we demonstrate that a strained Ge-rich SiGe alloy channel on sSOI is more beneficial to avoid dislocation introduction and to realize higher mobility than a Ge channel on the substrate. Pseudomorphically strained Ge-rich SiGe alloy ($Si_{0.1}Ge_{0.9}$) channel MOSFETs on sSOI substrate having a TaN / Si passivation / HfO_2 gate stacks were fabricated and a high effective hole mobility (μ_{eff} = 475 cm^2/Vs at N_s = 5.0x10^{12}cm^{-2}) and excellent subthreshold slope value (*S.S.* = 78 mV/dec.) were achieved simultaneously.

Device fabrication

Figure 1 shows a concept of proposed CMOS, featuring sSOI channel for nFET and strained (Si)Ge channel on sSOI for pFET. This architecture can enjoy the high mobility channels by simple process steps compared with local Ge condensation. Key fabrication steps of strained-(Si)Ge channel on sSOI MOSFETs are summarized in Fig. 2. Firstly, strained-Si channel was formed by mesa etching of sSOI (~1% biaxial tensile strain) substrates. Here, anisotropic strain relaxation of strained-Si mesa induced uniaxial stress along the channel direction to narrow fins. Then, hydrogen annealing at 850^{o}C was carried out to improve channel surface roughness and shrinkage of fin width. After that, strained-(Si)Ge channel and 1-nm thick Si passivation were grown by RPCVD at 380^{o}C only for pFETs. A 4 nm- HfO_2 layer was then grown by using an atomic layer deposition system. Figure 3 shows a xTEM of the narrowest channel with a core-Si width (W_{core}) of 28nm. It is clearly seen that smooth and circular shape of strained-Si core due to the effect of hydrogen annealing. Moreover, sidewalls of SiGe channel was mainly formed on the (111) facets. Figure 4 shows the comparison of xTEM between pure-Ge on sSOI and $Si_{0.1}Ge_{0.9}$ on sSOI. In pure-Ge on sSOI, dislocation which formed by strain relaxation was observed. On the other hands, dislocation formation is effectively suppressed in $Si_{0.1}Ge_{0.9}$ on sSOI by alleviation of lattice mismatch between shell and core materials. The W_{core} dependence of measured Raman peak shift, $\Delta\omega$ is shown in Fig.5(a). Extremely high (over -2.7%) compressive strain, which is almost identical with the misfit strain between $Si_{0.1}Ge_{0.9}$ and sSOI core, was evaluated at W_{core} = 145 nm. And comparison of remaining strain in channel direction, ε_{xx} in pure-Ge and $Si_{0.1}Ge_{0.9}$ channels ε_{xx} at biaxially strained wide $W_{core.}$ is shown in Fig.5(b). The $Si_{0.1}Ge_{0.9}$ channel has larger ε_{xx} than that for pure-Ge because of suppression of dislocation formation by alloy effect[12].

Hole-mobility characterization

Hole mobility was extracted by a split CV method for long-channel and multi-wire devices. N_s is the average surface carrier density defined by $N_s = N_l /(W_{top} +2 W_{edge})$, where N_l is the line inversion carrier density obtained from CV measurement. W_{top} and W_{edge} represent the wire width on top surface and length of faceted edges, respectively as shown in Fig. 4(a). Figure 6 shows the comparison of hole-mobility of the fabricated multi-wire MOSFETs. Here, $Si_{0.1}Ge_{0.9}$ on sSOI, $Si_{0.1}Ge_{0.9}$ on SOI and pure Ge on sSOI were used for comparative evaluation. Thanks to high compressive strain along the channel and less defective condition by avoiding strain relaxation, the $Si_{0.1}Ge_{0.9}$ on sSOI device show the highest mobility of 597 cm^2/Vs at N_s = 6.0x10^{12}cm^{-2} even though the mobility of pure Ge on sSOI was less than 360 cm^2/Vs. This result suggests that the advantage of $Si_{0.1}Ge_{0.9}$ in terms of the suppression of dislocation formation. Not only the current drive but the *S.S.* value was also improved as shown in Fig. 7. Figure 8 shows the effective hole mobility, μ_{eff} of anisotropically strained $Si_{0.1}Ge_{0.9}$ on sSOI MOSFETs with different core width, W_{core}. The mobility was decreased by shrinking W_{core}. Figure 9 shows the comparison of W_{core} dependence of peak mobility between strained $Si_{0.1}Ge_{0.9}$ on sSOI and $Si_{0.1}Ge_{0.9}$ on SOI pMOSFETs. At wide W_{core} region, mobility of $Si_{0.1}Ge_{0.9}$ on sSOI was increased with increasing W_{core} even though the mobility of strained $Si_{0.1}Ge_{0.9}$ on SOI core was almost unchanged. This mobility improvement can be explainable by the effect of anisotropic strain applied in $Si_{0.1}Ge_{0.9}$ on sSOI. On the other hands, at narrow W_{core} region, mobility was severely degraded at both devices. This effect might be due to the increased contribution of (111) sidewalls. To understand this strain and sidewall effect, "*thin*" strained $Si_{0.1}Ge_{0.9}$ on sSOI core pMOSFETs was evaluated. Figure 10 shows the comparison of W_{core} dependence of peak mobility, μ_{eff} for "*thick* (t_{SiGe} = 4~8 nm)" and "*thin* (t_{SiGe} = 2~6 nm)" anisotropically strained $Si_{0.1}Ge_{0.9}$ on sSOI pMOSFETs. The mobility enhancement by "*thin*" strained $Si_{0.1}Ge_{0.9}$ channel was also achieved. And almost same W_{core} dependency was observed. Figure.11 shows the comparison of W_{core} dependence of threshold voltage shift, ΔV_{th} between "*thick*" and "*thin*" strained-$Si_{0.1}Ge_{0.9}$ on sSOI. The V_{th} of "*thin*" strained $Si_{0.1}Ge_{0.9}$ was negatively shifted by decreasing W_{core}. This negative V_{th} shift can be attributable to the valence band energy modulation by changing the strain from biaxial to uniaxial. On the other hands, the V_{th} of "*thick*" strained $Si_{0.1}Ge_{0.9}$ was positively shifted by decreasing W_{core}. Moreover, subthreshold slope *S.S.* of "*thick*" strained $Si_{0.1}Ge_{0.9}$ was also degraded by decreasing W_{core} even though that for "*thin*" strained $Si_{0.1}Ge_{0.9}$ was improved (Fig. 12). These results suggest that the D_{it} at (111) sidewalls and/or hole generation in the channel deteriorate the *S.S.* values. And it might be suppressed by thinning the strained $Si_{0.1}Ge_{0.9}$ channel. In order to benchmark the performance for low-power operation, Fig. 13 shows a metrics of hole mobility enhancement factor against Si at N_s = 5x10^{12}cm^{-2} [13] versus subthreshold slope, *S.S.* value. The obtained combination of hole mobility enhancement factor of 7.7 against that of a Si counterpart and *S.S.* value of 78mV/dec. exhibits a potential to reduce the $|V_{dd}|$ lower than 0.5V with keeping a comparable intrinsic gate delay.

Conclusions

Anisotropically strained $Si_{0.1}Ge_{0.9}$ on sSOI pMOSFETs with high hole mobility and excellent *S.S.* values were demonstrated. The alloy channel was shown to be beneficial to prevent the lattice relaxation in spite of the high misfit strain. The obtained combination of hole mobility enhancement factor of 7.7 against that of a Si counterpart and *S.S.* value of 78mV/dec. exhibits a potential to reduce the $|V_{dd}|$ lower than 0.5V with keeping a comparable intrinsic gate delay. The result indicates that strained Ge-rich SiGe on sSOI pMOSFETs are promising for low-power sSOI-CMOS LSIs.

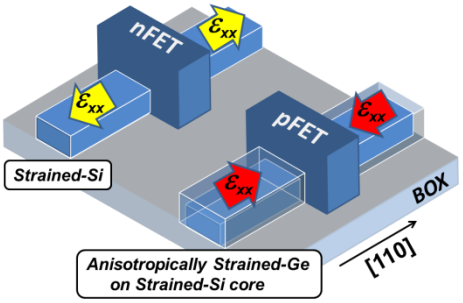

Fig. 1 Concept of proposed CMOS featuring sSOI nFET and strained-(Si)Ge / strained-Si channel pFET.

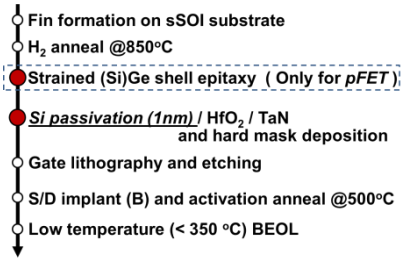

Fig. 2 Fabrication process of strained-Si core/ strained-(Si)Ge shell MOSFETs with Si passivation/HfO_2 gate stack.

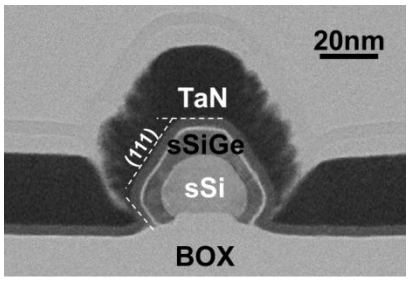

Fig. 3 Cross-sectional TEM image of strained $Si_{0.1}Ge_{0.9}$-shell on sSOI core with the narrowest core-Si width of 28nm.

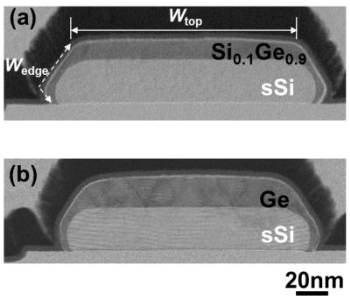

Fig. 4 Cross-sectional TEM images of **(a)** Ge on sSOI and **(b)** $Si_{0.1}Ge_{0.9}$ on sSOI after full processing. Dislocation formation in shell channel is effectively suppressed by Si incorporation.

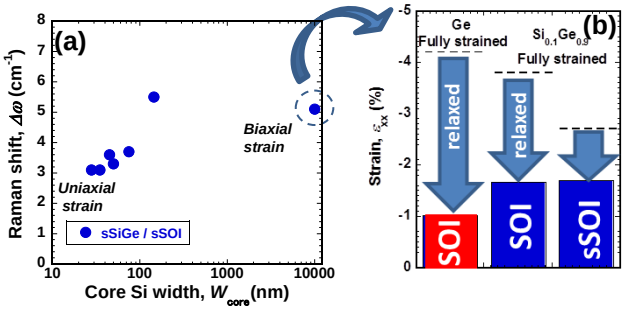

Fig. 5 (a) Measured Raman peak shift, Δω of Ge-Ge peak and **(b)** Comparison of remaining strain in channel direction, ε_{xx} in pure-Ge and $Si_{0.1}Ge_{0.9}$ channels ε_{xx} at biaxial strained wide W_{core}.

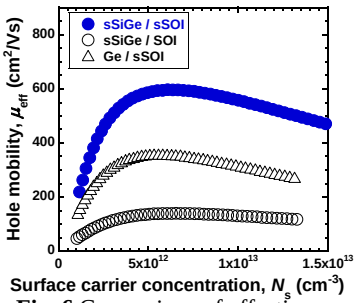

Fig. 6 Comparison of effective hole mobility, μ_{eff} of anisotropically strained (Si)Ge pMOSFETs (W_{core} = 145nm) with different cores.

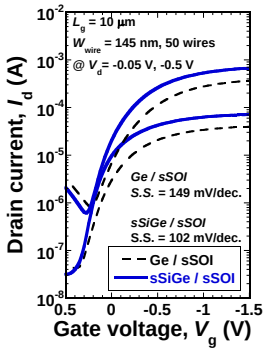

Fig. 7 Comparison of I_d-V_g characteristics of strained $Si_{0.1}Ge_{0.9}$ on sSOI and pure Ge on sSOI pMOSFETs.

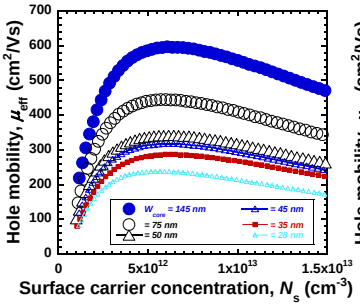

Fig. 8 Effective hole mobility, μ_{eff} of anisotropically strained $Si_{0.1}Ge_{0.9}$ on sSOI pMOSFETs with different core width, W_{core}.

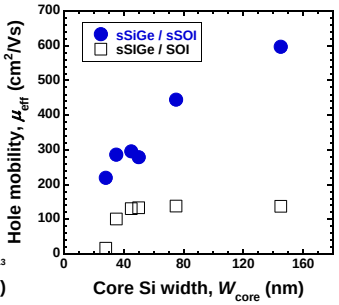

Fig. 9 Comparison of W_{core} dependence of peak mobility, μ_{eff} for strained $Si_{0.1}Ge_{0.9}$ on sSOI and strained $Si_{0.1}Ge_{0.9}$ on SOI pMOSFETs.

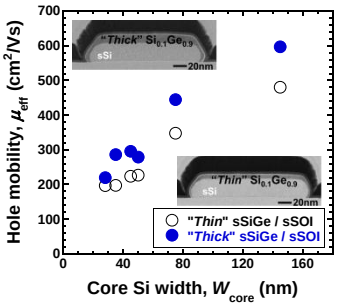

Fig. 10 Comparison of W_{core} dependence of peak mobility, μ_{eff} for "*Thick* (t_{SiGe} = 4~8 nm)" and "*Thin* (t_{SiGe} = 2~6 nm)" anisotropically strained $Si_{0.1}Ge_{0.9}$ on sSOI pMOSFETs.

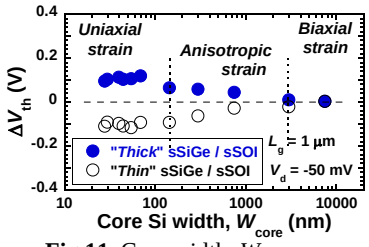

Fig.11 Core width, W_{core} dependence of linear threshold voltage shift, ΔV_{th}.

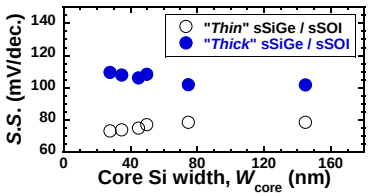

Fig.12 Core width, W_{core} dependence of subthreshold slope *S.S.*

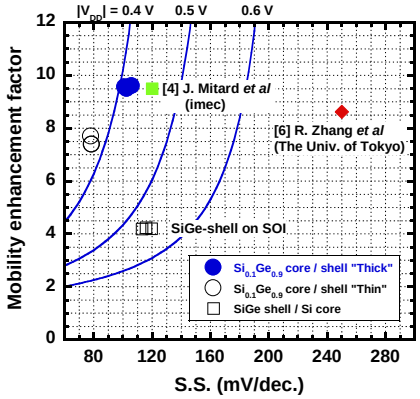

Fig.13 Benchmark of hole mobility enhancement factor with respect to MG/HK Si counterpart [13] vs *S.S.* Lines show required mobility enhancement at each $|V_{dd}|$. Larger mobility enhancement with lower *S.S.* can reduce $|V_{dd}|$ under the constant *CV/I*.

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