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Study of Si- and SiGe-on-Insulator Ω-gate Nanowire PMOS FETs by Low-frequency Noise Measurements

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Abstract

Low-frequency noise (LFN) has been investigated in Si and SiGe Ω-gate nanowire (NW) PMOS FETs. 3-types of technological splits have been studied, including reference Si-on-insulator (SOI), SOI with SiGe source/drain (S/D), and SiGe-on-insulator (SGOI). Our results reveal SGOI NW largely improves I_{ON} and is less impacted by S/D access resistance. Moreover, excellent quality of the oxide/channel interfaces with Hf-based high-k/metal gate is sustained in all the devices.

1. Introduction

Multigate (MG) architectures, such as NW FETs [1-4], are powerful solutions for upcoming CMOS technology nodes. In addition, the strain introduced for p-type channel by SiGe S/D [5] and/or SiGe channel [2,6] formation is a key feature for further enhancement of PMOS performance. However, controlled quality of the 3D multiple interfaces with strain effect could be a critical issue. LFN measurement is an efficient diagnosis tool to assess the electrical properties of FETs, even in aggressively scaled MG architectures [2,7-10]. In this work, the oxide/channel interface properties are investigated in detail by LFN characterization for SOI and SGOI Ω-gate NW PMOS FETs.

2. Devices, Measurements, and Results

The Ω-gate NW PMOS FETs (Fig.1) were fabricated starting from (001) SOI wafers with ≈12nm-thick Si (corresponding to the NW height H_{NW}), and 145nm-thick BOX, using the top-down approach [3,4]. Compressive strain has been introduced to the channel by $Si_{0.8}Ge_{0.2}$ channel formed by Ge enrichment technique and/or by raised $Si_{0.7}Ge_{0.3}$ S/D. The initial biaxial stress in SGOI corresponds to ≈1.2GPa and is reduced to a uniaxial stress in NWs. After etching, [110]-oriented NW structures with top width W_{top} down to ≈14nm have been obtained. All the devices have a HfSiON/TiN gate stack leading to EOT=1.25nm. The I_d-V_g curves of the narrowest NW FETs show good properties for all the technological splits (Fig.2). SGOI NW demonstrates I_d enhancement as high as ≈+170% compared to SOI NW.

LFN measurements were performed at room temperature under a probe level using a semi-automatic noise measurement system by Synergy concept [11]. Normalized drain current noise spectra S_{Id}/I_d^2 as a function of frequency in the SOI and SGOI narrowest NWs show 1/f noise behavior at the threshold voltage operation (Fig.3). 1/f noise can be interpreted by the CNF+CMF model (cf. (2) in Table I) [12,13] as for NMOS NWs [9,10]. Fig.4 shows the S_{Id}/I_d^2 spectra normalized by the channel area (W_{tot} and L_g), as a function of I_d for all our devices. Agreement between the S_{Id}/I_d^2 plots and the corresponding $(g_m/I_d)^2$ curves is observed in all the devices. For SOI devices, a large roll-up of the noise level in strong inversion for both NW and wide FETs is also observed. This indicates the contribution from S/D series resistance R_{SD} [14]. The worse S/D contact for PMOS than NMOS is generally attributed to less controllability of the boron dopant. The CNF+CMF model can be simply completed by considering the excess noise stemming from the S/D access region as (3) in Table I [14]. In Fig.5, the S_{Id}/I_d^2-I_d plots above V_t for SOI devices can be perfectly described by R_{SD} impact. For both SiGe S/D and SGOI, the spectra in the NWs are well interpreted by considering both $\alpha_{sc}\mu_{eff}$ and S_{Rsd} terms, whereas for wide FETs the $\alpha_{sc}\mu_{eff}$ term is dominant. The summarized $\alpha_{sc}\mu_{eff}$ and S_{Rsd} values clearly show the advantage of SGOI devices, and also agree with better R_{SD} value for NWs. Extracted S_{Vfb} by direct fitting method [9] exhibits roughly simple channel scaling effect, *i.e.* the noise level is inversely proportional to W_{top}, for all the splits (Fig.6). The gate oxide trap density N_t around quasi-Fermi energy level can be derived using S_{Vfb} as (4) in Table I [13]. The computed N_t values lie in same order for all the splits and in similar or lower order as previous reports regardless of the carrier type [5,8-10], and are not significantly altered by the W_{top} scaling and the NW geometry (Fig.7a). It is concluded that excellent oxide/interface quality is maintained in all the Si and SiGe channel devices down to the narrowest NW FETs. The contributions of top surface (Nt_top) and side-wall (Nt_side-wall) can further be assessed [9] (Fig.7b). The (110) planes in side-walls are slightly better than the (100) top surface in all the devices, whereas strain technology does not largely degrade the interface quality.

3. Conclusions

The oxide/channel interface in ultra-scaled Ω-gate NW PMOS FETs have been analyzed by LFN measurements. The CNF+CMF model with consideration of R_{SD} impact perfectly assesses 3-types of technological variants. An excellent quality of the interface, with oxide trap density below $5\times10^{17}eV^{-1}cm^{-3}$, is preserved for all the devices down to the narrowest NWs. We thus demonstrated that SGOI NW has powerful potential for high PMOS performances with significant I_{ON} enhancement compared to SOI NW, while maintaining low R_{SD} and good interfaces.

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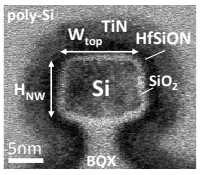
Table I. Considered equations in this paper

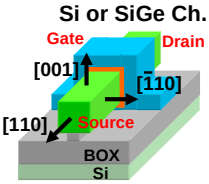
$$W_{tot} = W_{top} + 2H_{NW} \quad (1)$$

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 \left(1+\alpha_{sc}\mu_{eff}C_{ox}\frac{I_d}{g_m}\right)^2 S_{Vfb} \quad (2)$$

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 \left(1+\alpha_{sc}\mu_{eff}C_{ox}\frac{I_d}{g_m}\right)^2 S_{Vfb} + \left(\frac{I_d}{V_d}\right)^2 S_{Rsd} \quad (3)$$

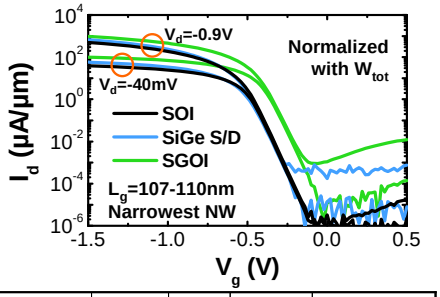
$$N_t = \frac{fW_{tot}L_g C_{ox}^2 S_{Vfb}}{q^2 kT\lambda} \quad (4)$$





[110]-oriented Ω-gate PMOS	Channel	Raised S/D with B dope	NW height H_{NW}	Narrowest NW top width W_{top}	Gate length L_g
SOI	Si	Si	13.5nm	17nm	107nm
SiGe S/D	Si	$Si_{0.7}Ge_{0.3}$	9.5nm	14nm	110nm
SGOI	$Si_{0.8}Ge_{0.2}$	$Si_{0.7}Ge_{0.3}$	11.5nm	13nm	108nm

Fig. 1. Schematics of the Ω-gate NWs and TEM picture of the cross-section of SOI NW. The table summarizes the technological splits.



[110]-oriented Ω-gate NW	V_t (V) V_d=-40mV	DIBL (mV/V)	SS (mV/dec)	I_{ON} gain vs. SOI V_g=V_t=-0.9V
SOI	-0.48	~23	60.9	133 µA/µm
SiGe S/D	-0.5	~47	63.6	+21%
SGOI	-0.4		68.2	+166%

Fig. 2. I_d-V_g curves of the narrowest NW FETs for all the technological splits, and table summarizing the basic performances of the FETs.

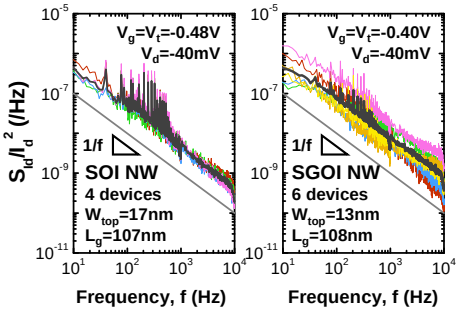


Fig. 3. Normalized drain current noise S_{Id}/I_d^2 as a function of frequency in the narrowest NW FETs for (a) SOI and (b) SGOI devices (bold line: average on 4 or 6 devices).

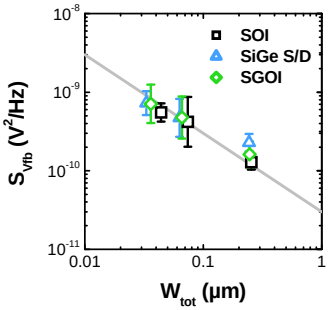


Fig. 6. Flat-band voltage noise S_{Vfb} as a function of the total effective channel width W_{tot} for all the devices.

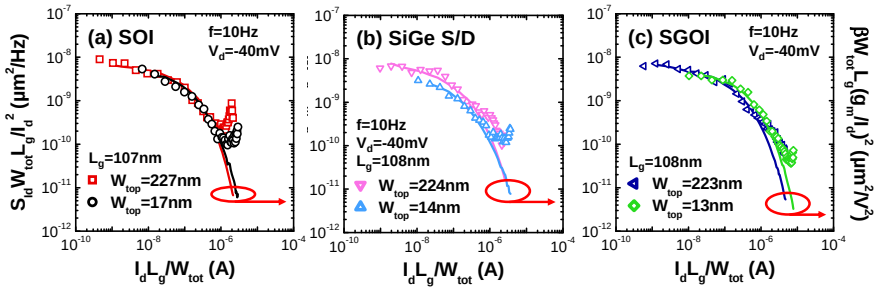
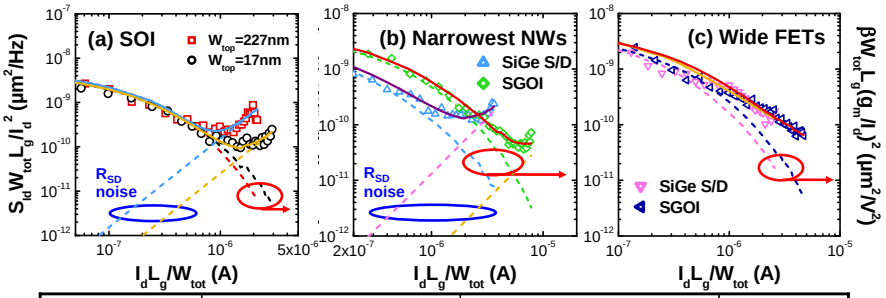


Fig. 4. I_d dependent (symbols) drain current noise S_{Id}/I_d^2 and (lines) corresponding $(g_m/I_d)^2$ curve characteristics normalized by channel area parameters (W_{tot} and L_g) for the narrowest NW and wide FETs in (a) SOI, (b) SiGe S/D, and (c) SGOI devices.



[110]-oriented Ω-gate PMOS	$\alpha_{sc}\mu_{eff}$ (×10⁶ cm²/C)		S_{Rsd} (Ω²/Hz)		R_{SD} (Ω µm)
	Wide	NW	Wide	NW	NW
SOI	No impact	No impact	1.6	50	173
SiGe S/D	1.5	1.1	No impact	65	172
SGOI	1.4	0.75	No impact	1.7	104

Fig. 5. I_d dependent (symbols) S_{Id}/I_d^2 and (lines) corresponding $(g_m/I_d)^2$ curve with consideration of the $\alpha_{sc}\mu_{eff}$ and S_{Rsd} term shown in (2), showing (a) the narrowest NW vs. wide FETs in SOI devices, and SiGe S/D vs. SGOI devices in (b) NWs, and in (c) wide FETs. The table summarizes the extracted $\alpha_{sc}\mu_{eff}$ and S_{Rsd} values for all the PMOS FETs, and the S/D series resistance R_{SD} in NWs.

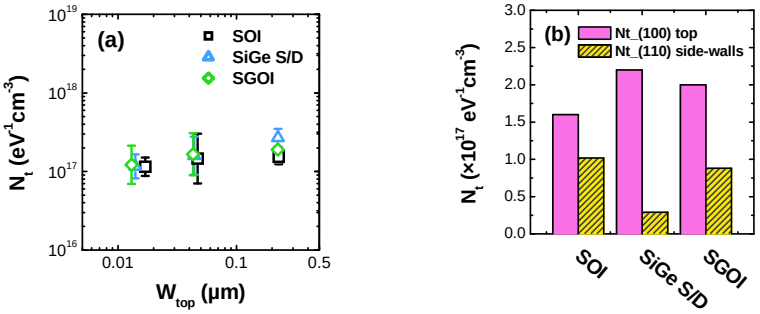


Fig. 7. (a) Gate oxide trap density N_t as a function of the channel top width W_{top} for all the devices. (b) Extracted N_t components of the channel top surface and side-walls by a model of the contributions separation [9].