Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp866-867

Ultra Low-Frequency Noise in Vertical MOSFETs Having Tunable Threshold Voltage Fabricated with 60 nm CMOS Technology on 300 mm Wafer Process

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Abstract

We successfully fabricated n-type and p-type vertical MOSFETs (V-MOSFETs) with 60 nm CMOS technology on 300 mm wafer process. It is demonstrated that fabricated n-/p-type V-MOSFETs achieve excellent subthreshold swing of 69 mV/dec. / 66 mV/dec. and I_{on}/I_{off} ratio of $1x10^7/2x10^6$ with having tunable threshold voltage (V_{th}) from 0.26 V to 0.40 V. This tunable V_{th} is difficult for previous nanowire type MOSFETs. Back bias effect is also successfully eliminated due to the body isolation from silicon substrate. Moreover, it is demonstrated that V-MOSFETs can suppress low-frequency noise (1/*f*) ($L_{gate}WS_{id}/I_d^2$ of 10^{-13}~10^{-11} μm²/Hz for n-type and 10^{-12}~10^{-10} μm²/Hz for p-type). This 1/*f* of fabricated V-MOSFET is drastically one or two order lower than previously reported multi-gate and planar MOSFETs.

1. Introduction

Vertical MOSFETs (V-MOSFETs) are considered to be the most attractive devices for ultralow power LSI, due to their excellent gate controllability with gate-all-around structures [1,2]. In addition, V-MOSFETs achieve high area efficiency of circuit because V-MOSFETs can combine layout space for source, body and drain. On the other hand, low-frequency (1/*f*) noise in MOSFETs is becoming more important factor as device size and supply voltage (V_{DD}) is scale down [3,4]. Therefore, suppressing 1/*f* noise is strongly required for future ultra-low power LSI. In this work, we demonstrate low-leakage n-type and p-type Vertical MOSFETs fabricated on 300 mm wafer process with 60 nm diameter for the first time. Moreover, 1/*f* noise of V-MOSFETs is also investigated for the first time.

2. Devices and Measurement setup

The V-MOSFETs (Fig.1) were fabricated on 300 mm silicon wafer. In this work, bottom node diffusion layer is used as source and top node is used as drain terminal. Silicon pillar diameter (D_{Pillar}) is 60 nm, gate length (L_{gate}) is 100 nm, and *EOT* is 3 nm (Table I). 1/*f* noise measurements were carried out at 25 degree C under a probe level using *Agilent* noise measurement system. The drain current noise (S_{id}) were measured at V_{GS} = 1.0 V and V_{DS} = 50 mV.

3. Measurement Results and Discussion

3-1. DC performances of Vertical MOSFETs

The measured I_D-V_{GS} characteristics of n- and p-type V-MOSFETs achieved suppressing short channel effect as shown in Fig.2. *DIBL* is only 34 mV/V for n-type and 66 mV/V for p-type. Steep subthreshold swing (*SS*) is achieved and 69 mV/dec. for n-type and 66 mV/dec. for p-type. Thanks to the low *DIBL* and steep *SS*, low off-leakage current (I_{off} = 5.3 pA for n-type and 15 pA for p-type) is achieved. Fig.3 shows the measured I_D-V_{DS} characteristics of n- and p-type V-MOSFETs. On current (I_{on}) is 53 μA for n-type and 28 μA for p-type. I_{on}/I_{off} ratio is achieved $1x10^7$ for n-type and $2x10^6$ for p-type, respectively. The measured I_D-V_{GS} characteristics with three different channel doping condition are shown in Fig.4. Threshold voltage (V_{th}) can be controlled with maintaining *SS* by channel doping concentration. I_{on}-I_{off} characteristics (169 samples) are shown in Fig.5. Both n- and p-type V-MOSFETs are achieved the tunable V_{th}. In addition, the back bias effect is eliminated as shown in Fig.6(a). Substrate voltage (V_{SUB}) is biased from -0.5 V to 0.5 V. DC performances of V-MSOFETs are independent of V_{SUB}, because the body region is isolated by bottom diffusion layer.

3-2. 1/*f* noise performances of Vertical MOSFETs

Fig.6(b) shows the S_{id} normalized by I_D (S_{id}/I_d^2) of n-type V-MOSFETs with V_{SUB} ranges from -0.5 V to 0.5 V. It has been reported that 1/*f* noise depends on substrate bias in the bulk planar MOSFET or bulk FinFET [5,6]. On the other hand, in the V-MOSFETs, thanks to the eliminated back bias effect, S_{id}/I_d^2 is also independent on V_{SUB}. Figs.7 and Figs.8 are S_{id}/I_d^2 characteristics of n- and p-type V-MOSFETs with three different *Vth*. These data were measured from 5 samples with the same size of D_{Pillar}/L_{gate} = 60 nm/100 nm. Thick solid lines indicate the averaged values. The averaged S_{id}/I_d^2 of both n- and p-type V-MOSFETs follows 1/*f* law. Averaged S_{id}/I_d^2 at 100 Hz is extracted and normalized by channel area ($L_{gate} \times W$) as shown in Fig.9. In this study, *W* is defined as the circumference of silicon pillar ($\pi \times D_{Pillar}$). The $L_{gate}WS_{id}/I_d^2$ of p-type V-MOSFET is larger by about ten times than n-type V-MOSFET. Fig.9 shows comparison of $L_{gate}WS_{id}/I_d^2$ at 100 Hz with other previously reported device structures [7-9]. From these results, it is demonstrated that V-MOSFETs can suppress 1/*f* noise to one or two order lower than previously reported nanowire, FinFET, Tri-Gate, and planar MOSFET.

4. Conclusions

We successfully fabricated V-MOSFETs with 60 nm CMOS technology on 300 mm wafer process. The fabricated V-MOSFETs achieved tunable V_{th} with excellent device DC performance and ultra-low 1/*f* noise as shown in Table I. The ultra-low 1/*f* of V-MOSFET with tunable V_{th} is useful for low voltage LSI such as high density memory cell with small signal and small footprint.

Acknowledgements: This work has been supported in part by JST, ACCEL, and CREST under JST.

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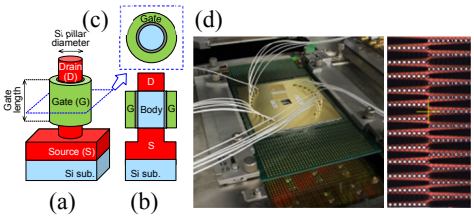

Fig.1. Description of the V-MOSFETs and measurement setup studied in this paper. (a) bird's eye view, (b) cross-sectional view, (c) vertical-sectional view, and (d) picture image of TEG in a wafer. Bottom node is used as source, and top node is used as drain.

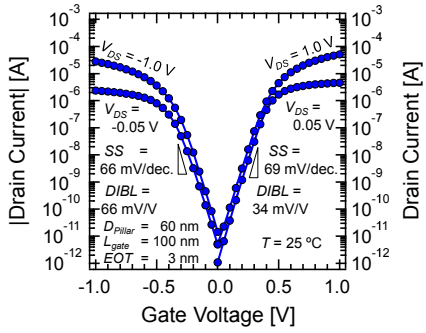

Fig.2. I_D-V_{GS} characteristics of both the n- and p-type V-MOSFETs. Suppressed *DIBL* (< 70 mV/V), steep subthreshold swing (< 70 mV/dec.), and low off-leakage current (10^{-12}~10^{-11} A) are achieved.

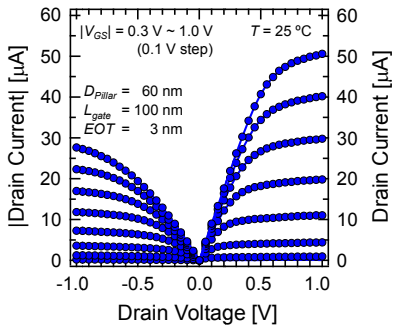

Fig.3. I_D-V_{DS} characteristics of both the n- and p-type V-MOSFETs. On current (I_{on}) is 53 μA for n-type and 28 μA for p-type. I_{on}/I_{off} of 1x10^7 for n-type and 2x10^6 for p-type are achieved.

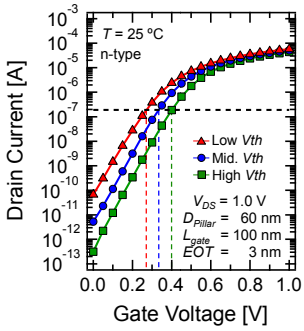

Fig.4. I_D-V_{GS} characteristics with three different channel doping condition of n-type. Tunable threshold voltage (V_{th} = 0.26 V ~ 0.40V) is achieved with steep *SS*.

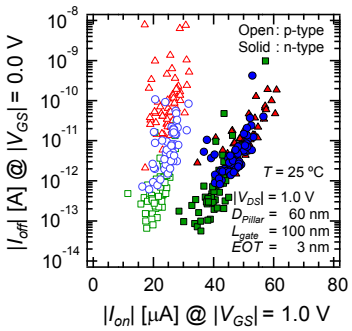

Fig.5. I_{on}-I_{off} characteristics of both the n- and p-type V-MOSFETs (169 samples for each type). The data which I_{on} is less than 20 μA for n-type and 10 μA for p-type is excluded.

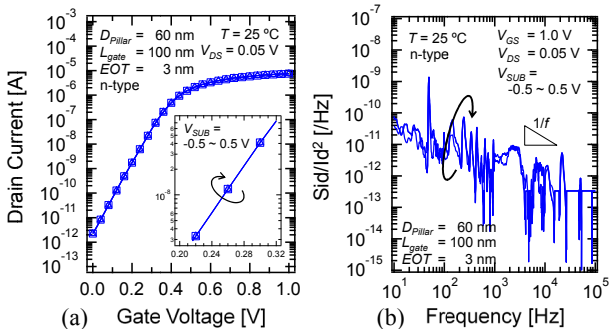

Fig.6. Back bias effect on (a) DC performance and (b) low-frequency noise (1/*f*). Back bias effects on both characteristics are successfully eliminated due to the body isolation from silicon substrate by using bottom node diffusion layer (source) as shown in Fig.1(c).

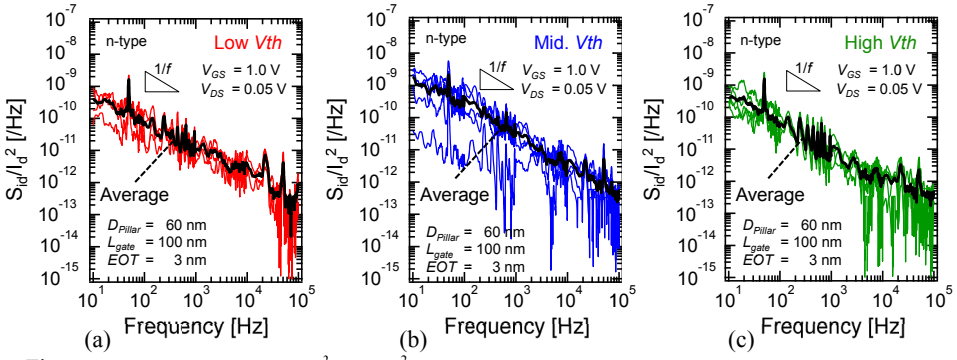

Fig.7. Normalized S_{id} by I_d^2 (S_{id}/I_d^2) as a function of frequency of fabricated n-type V-MOSFETs for three different V_{th} (V_{GS} = 1.0 V and V_{DS} = 0.05 V). (a) Low V_{th}, (b) Middle V_{th}, and (c) High V_{th}. Thick solid lines indicate the averaged values of 5 samples.

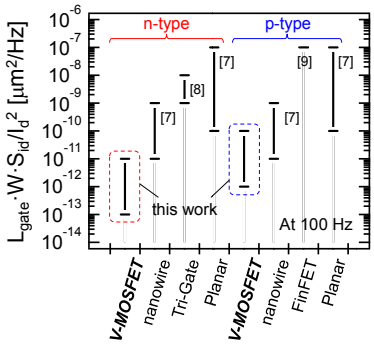

Fig.9. Comparison of normalized S_{id}/I_d^2 by L_{gate} × W at 100 Hz. W is defined as the circumference of silicon pillar (π × D_{Pillar}). V-MOSFETs can suppress 1/*f* noise to one or two order smaller than previously reported nanowire type MOSFET, FinFET, Tri-Gate, and planar MOSFETs.

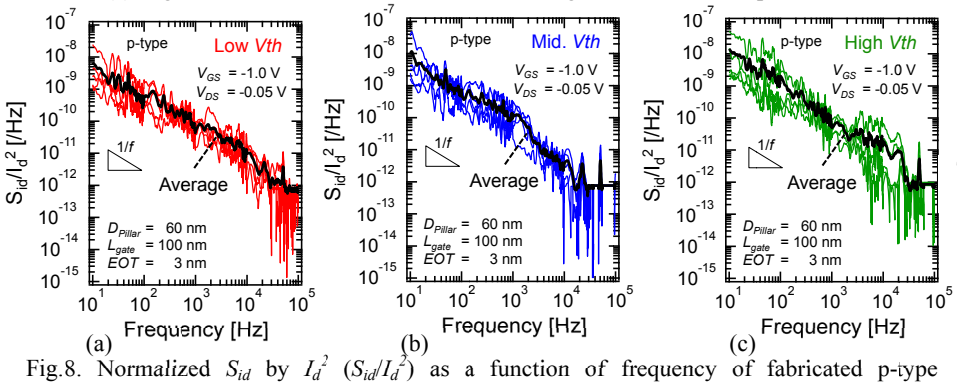

Fig.8. Normalized S_{id} by I_d^2 (S_{id}/I_d^2) as a function of frequency of fabricated p-type V-MOSFETs for three different V_{th} (V_{GS} = 1.0 V and V_{DS} = 0.05 V). (a) Low V_{th}, (b) Middle V_{th}, and (c) High V_{th}. Thick solid lines indicate the averaged values of 5 samples.

Table I. Measurement results of fabricated n-/p-type V-MOSFETs.

parameters	n-type	p-type
D_{Pillar} [nm]	60	
L_{gate} [nm]	100	
EOT [nm]	3	
SS [mV/dec.]	69	66
V_{th} [V]	0.26 ~ 0.40	-0.23 ~ -0.41
I_{on} [μA] @ I_{off} = 1 pA	40	25
L_{gate}·W·S_{id}/I_d^2 [μm²/Hz]	10^{-13} ~ 10^{-11}	10^{-12} ~ 10^{-10}