Comprehensive Studies on the Accuracy of Traps Characterization by Using Advanced Random Telegraph Noise Simulator

Y. Higashi, K. Matsuzawa and T. Ishihara

Advanced LSI Technology Laboratory, Corporate R&D Center Toshiba Corporation, Kawasaki, 212-8582, Japan Phone: +81-44-549-2316 E-mail: yusuke.higashi@toshiba.co.jp

Abstract

Our developed noise simulator can represent the dynamic behavior of electron and hole trapping and de-trapping via interactions with both the Si substrate and Poly-Si gate. Simulations reveal that the conventional analytical model using the ratio between the capture and emission time constants yields large errors in the estimates of trap site positions due to interactions with the Si substrate and Poly-Si gate.

1. Introduction

In recent years, many experimental results for the trap time constants of random telegraph noise (RTN) have been reported [1, 2]. Nagumo et al. [1] reported the existence of trap sites which exchange carriers with the gate electrode instead of the Si substrate. This result indicates that an RTN simulator needs to simultaneously reproduce trapping and de-trapping behavior through interactions with both the Si substrate and also the gate. Nagumo et al. [1] also reported no correlation between the trap time constants and the distance from the Si substrate to the trap site, which contradicts the conventional model of flicker noise [3]. Mauri et al. [4] argued that atomistic doping effects yield a spread out distribution of trap time constants mainly due to non-uniform channel inversion. However, this has not been able to sufficiently explain the measured distribution of trap time constants.

2. Simulation Results and Discussions

The transient noise simulation (TNS) model is shown schematically in Fig.1. Discretized traps are arranged randomly in the real and energy spaces [5, 6]. Trapping and de-trapping processes are made to occur by using a Monte Carlo method based on the capture time constant τ_c and emission time constant τ_e of each trap. We consider energy transitions based on the multiphonon-assisted model [7, 8, 9]. The model proposed by Herrmann and Schenk [8] reproduces only trapping from the Si substrate and de-trapping to the Poly-Si gate in order to calculate the trap-assisted tunneling current. For RTN simulation, we extended the model to reproduce the behavior of de-trapping to the Si substrate and trapping from the Poly-Si gate [9]. Figure 2 shows the $\Delta I_{ds}/I_{ds}$ waveforms obtained by TNS for a large size (L=1.0 µm and W=1.0 µm) and a smaller size nMOSFETs (L=0.1 µm and W=0.1 µm). In smaller devices, the mean number of traps is smaller and single trap events therefore occur more frequently. In addition, the mean value of $\Delta I_{ds}/I_{ds}$ becomes larger because number of carriers decrease and single trap charge effect becomes larger.

Figure 3 shows the dependence of τ_c and τ_e on gate voltage. Various different combinations of trap site position and energy level are shown. For trap site near the Si substrate (Fig. 3(a)), τ_c decreases with higher applied gate voltage because the trap site energy level is lower than the quasi Fermi energy of the Si substrate. For trap site near the Poly-Si gate (Fig. 3(b)), τ_c increases with higher applied gate voltage because the trap site energy level is higher than the quasi Fermi energy of the Poly-Si gate. For trap site in the middle (Fig. 3(c)), τ_c changes by only a small amount because the middle position is affected by the Si from both sides. Figure 4 shows the dependence of the τ_c/τ_e ratio on the gate volt-

age. In several papers, trap site positions have been calculated using the following equation [1]:

$$\frac{Z_{t}}{T_{cr}} = -\frac{kT}{q} \frac{\partial \ln(\tau_{c} / \tau_{e})}{\partial V_{e}}$$
(1),

where q, k, T are the elementary charge, the Boltzmann constant and the temperature. In the above equation, a small gradient in the τ_c/τ_e ratio gives a small value of Z_t . However, the trap sites in middle positions between the Si substrate and Poly-Si gate exhibit a small gradient in the τ_c/τ_e ratio due to capture and emission interactions with both Si sides as shown in Fig. 4(c). This shows that the trap site positions may be miscalculated when estimated using Eq. (1). Figure 5 shows trap sites positions in real and energy spaces for Fig. 3 (a), (b), and (c). The effect of the interaction of Si substrate and Poly-Si gate are very sensitive to trap sites position in real and energy spaces. Figure 6 shows the actual trap site positions Z_{t-real} used in the TNS versus the calculated positions Z_{t-calc} from Eq. (1) for the 180,000 randomly arranged trap sites. As discussed above, the values of Z_{t-calc} near the middle position of Z_{t-real} in the vicinity of 2 nm were miscalculated as being near the Si substrate or Poly-Si gate. Figure 7 shows the time constant τ_0 ($\tau_0 = \tau_c = \tau_e$) versus Z_{t_real} and Z_{t_calc} . Although τ_0 exhibits exponential dependence on Z_{t-real} due to the tunneling probability in Fig. 7(a), in Fig. 7(b) τ_0 is widely distributed in Z_{t-calc} space due to the miscalculation. The method of calculating Z_t using Eq. (1) therefore needs to be implemented carefully in order to avoid this kind of miscalculation. Figure 8 shows estimated lower limit of τ_0 for trap sites at middle position in gate insulator. The miscalculations occur more readily in thin gate-insulator MOSFETs whose lower limit is in the RTN measurement region. In thick gate insulator MOSFETs, $T_{ox} > 5.5$ nm, the interaction with the Si substrate and Poly-Si gate becomes negligible because τ_c and τ_e of opposite silicon sides are longer than the RTN measurement time.

3. Conclusion

We found that the conventional analytical model yields estimates of trap site positions with large errors due to interactions with the Si substrate and Poly-Si gate sides, particularly in thin gate-insulator MOSFETs, and obtained the gate-insulator thickness to avoid the miscalculation due to the interaction with the both silicon sides.

References

[1] T. Nagumo et al., in IEDM Technical Digest, p.628, 2010.[2] A. Yonezawa et al., in IEEE International Reliability Physics symposium, p.3B.5.1, 2012. [3] M. J. Kirton, and M. J. Uren, Advences in Physics, 38, p.367, 1989. [4] A. Mauri et al., in IEDM Technical Digest, p.405, 2011. [5] K. Matsuzawa, T. Ohguro, and N. Aoki, in International Conference on Simulation of Semiconductor Processes and Devices, p.83, 2003.[6] Y. Higashi et al., in Symposium on VLSI Technology Digest of Technical Papers, p.200, 2011.[7] B. K. Ridley, Quantum Processes in Semiconductors, 1999.[8] M. Herrmann and A. Schenk, J. Appl. Phys. 77, p.4522, 1995. [9] Y. Higashi et al., IEEE Trans. ED, submitted for publication.





Fig. 2 Simulated $\Delta I_{ds}/I_{ds}$ waveform. T_{ax} =4nm, N_r =1 × 10¹⁷ cm⁻³ eV⁻¹ . V_g = V_r , V_d =1.0 V, (a) L=W=1 μ m, (b) L=W=0.1 μ m. (b) show the random telegraph signal noise due to a single trap events.

Fig. 1 Schematic of TNS model for nMOSFET. Discretized traps are arranged randomly in real and energy spaces. Electrons tunnel to the trap position via multiphonon-assisted energy transitions.



Fig. 3 Simulated gate voltage dependence of τ_c and τ_c , T_{ox} =4nm, L=W=0.1 µm, (a) for trap site near the Si substrate, Z_r =1.2nm, E_r =0.9eV, (b) for trap site near the Poly-Si gate, Z_r =2.7nm, E_r =0.3eV, and (c) for trap in the middle, Z_r =1.7nm, E_r =0.6eV.



4 3.5 9 9 9 1.5 0.5 1.1.5 2.2.5 3.3.5 4 2 2.cea[m]

Fig. 6 The actual trap site positions $Z_{t real}$ vs. the calculated positions $Z_{t calc}$ for the 180,000

randomly arranged trap sites.

Fig. 4 Simulated gate voltage dependence of the τ_c/τ_e ratio, T_{ox} =4nm, L=W=0.1 µm, (a) for trap site near the Si substrate, Z_i =1.2nm, E_i =0.9eV, (b) for trap site near the Poly-Si gate, Z_i =2.7nm, E_i =0.3eV, and (c) for trap site in the middle, Z_i =1.7nm, E_i =0.6eV.



10 middle Z_t [sec] 10 Lower measurement 1 region = error affecting limit region 10- τ_o at I 10 10 2 3 4 5 6 7 T_{ox} [nm]

Fig. 7 (a) Z_{t_real} vs. τ_0 (b) Z_{t_calc} vs. τ_0 (a) τ_0 exhibits exponential dependence on Z_{t_real} due to the tunneling probability equation. (b) τ_0 is widely distributed in Z_{t_calc} space due to the miscalculation using Eq. (1).

Fig.8 Estimated lower limit of τ_0 for trap sites at middle position of gate insulator.

Fig.5 Trap sites position in real and energy spaces for Fig.3(a),(b),and (c) .