Flip-Flop circuits using fully solution processed pseudo-CMOS circuits

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Abstract

Organic flip-flop (FF) circuits based on pseudo-CMOS inverters have been fabricated by fully solution-processes. Bottom-gate, bottom-contact organic thin-film transistors using a solution-processable small molecular semiconductor exhibited an average mobility $0.35 \text{ cm}^2/\text{Vs}$. The fabricated FF circuits were successfully operated in ambient air condition and exhibited a short delay time (3.5 ms) at a supply voltage of $\pm 20 \text{ V}$.

1. Introduction

Organic Thin Film Transistor (OTFT) is very attractive for a varied range of applications such as flexible display, sensor and radio-frequency identification (RFID) tags because Organic materials possess intrinsic mechanical flexibility and solubility in organic solvents. Solution-processes make possible to use printing technologies that are appropriate for large area flexible film substrates and thus for ultra-low-cost electronic device. However, the level of performance achieved by organic integrated circuits fabricated using solution / printing process is still not sufficient to enable practical application. The main reason for this is the relatively long channel length caused by the limited resolution of printing methods. Furthermore, complementarity circuits using both p-type and n-type semiconductors fabricated entirely with printable processes have generally not been able to achieve a high signal gain. The primary reason for this is that, because solution-processable n-type semiconductor materials with a high mobility have been developed in recent years, their performance in OTFT devices remains lower than those of p-type semiconductor materials. Accordingly, it has been difficult to fabricate high-performance complementary circuits using a combination of printable p-type and n-type organic semiconductor materials. Therefore, it is very important to be able to fabricate organic integrated circuits using OTFT with only p-type semiconductor. In our previous work, we presented fully solution-processed pseudo-CMOS inverter and NAND / NOR circuit with polymer semiconductor $\ensuremath{^{[1]}}$. In this work, we have fabricated a RS-flip flop (FF) circuits by integrating fully solution-processed pseudo-CMOS inverter^[2] using a small molecules semiconductor. We have successfully demonstrated a RS-FF circuit in ambient air condition with excellent input-output performance at supply

voltage of ± 20 V, and delay time of 3.5 ms.



Fig. 1 Schematic illustration of a fabricated OTFT.

2. Experimental

Cross-section of the OTFT fabricated in this work is shown in Fig. 1. Bottom-gate, bottom-contact OTFT devices were fabricated entirely with solution processes. A ink-jet printer (model DMP-2831, Dimatix Corp.) was used to form the silver electrodes. A cross-linked polyvinylphenol (PVP) was used as a base layer. PVP ($M_w \sim 25000$) and poly(melamine-co-formaldehyde) as a cross-linking agent were mixed in propylene glycol monomethyl ether acetate (PGMEA). The PVP solution was spin-coated and was thermally cross-linked at a temperature of 150°C for 60 min in a nitrogen atmosphere to form a base layer. The base layer was then treated with oxygen plasma for controlling wetting properties. The water-based silver nanoparticle ink (JAGLT series, DIC Co.) was patterned onto a base layer to form gate electrode. Following the printing, the substrate were stored under controlled temperature and humidity conditions in order to planarize the gate electrode^[3]. After the drying process, the substrates were sintered at 140°C for 30 min in ambient air. The PVP solution was spin-coated and cured under same conditions to from a 490 nm thick gate dielectric layer. The hydrocarbon-based silver nanoparticle ink (NPS-JL, Harima Chemicals, Inc.) was patterned onto the gate dielectric layer to form source/drain electrodes. After the printing, the substrates were sintered at 120°C for 30 min in ambient air. Next, a solution amorphous fluoropolymer (Teflon[®] AF1600, DupontTM) in FLUORINERTTM (FC-43, 3M Co.) was patterned using a dispenser system (IMAGEMASTER 350PC, Musashi Engineering, Inc.) to create bank layers for separation of the organic semiconductor layer. Before the deposition of semiconducting layer, the source / drain electrode surfaces were treated with a pentafluoro-benzenthiol

(PFBT) solution to form self-assembled monolayer^[4]. Finally, a mesitylene-based solution of an organic semiconductor (lisicon® S1200, Merck) was printed into the area defined by the bank layer by using dispenser equipment^[5]. After patterning the semiconducting layer, the substrates were baked at 100°C for 1 min on a hotplate. Using the same procedure as the OTFT fabrication, we have fabricated a RS-FF circuit.

3. Results and Discussions

Fig. 2 shows Transfer and output characteristics of fabricated OTFT with channel length 59 µm and width 364 µm. The OTFT exhibited a field-effect mobility of 0.4 cm²/Vs in the saturation region, an on/off current ratio of 10^4 , a threshold voltage of -2.4 V. The linearity at low voltages suggests good electrical contact between the printed silver electrodes and organic semiconductor layer. The work function of printed Ag electrode was 4.7 eV and it increased to 5.4 eV by PFBT formation. The increase of the work function decreases the charge injection barrier to the organic semiconductor from the printed Ag electrode. Fig. 3 shows distributions of various mobility and threshold voltage values. The average mobility in the saturation regime was $0.35 \text{ cm}^2/\text{Vs}$ (standard deviation: 0.14), and the average threshold voltage was -2.2 V (standard deviation: 1.3). This variation extremely affects the performance of the inverter.



Fig. 2 (a) Transfer and (b) output characteristics of fully solution-processed OTFT in the saturation regime.



Fig. 3 Threshold voltages and mobility as measured from 48 TFTs

A NAND-based RS-FF as shown in Fig. 4(a) was designed. Each two-input NAND gate consists of six transistors, and the FF consists of 12 transistors in total. At this time, in order to reduce the variation of transistor characteristics, we designed a new type of transistor where six transistors are arranged in parallel to average the transistor characteristics. We could easily fabricate the new transistors because the printing processes are on-demand. Fig. 4(b) shows a photograph of the fabricated device. Fig. 5 shows input-output characteristics of the RS-FF at supply voltage (V_{DD}) of 20 V and a tuning voltage (V_{SS} = $-V_{DD}$). The RS-FF circuit exhibited a characteristic according to truth table at low operating voltage. A measured total delay time for the RS-FF was 3.5 ms at 20 V and 6.4 ms at 10 V.



Fig. 4 (a) Circuit diagram and (b) optical image of a RS-FF.



Fig. 5 input-output characteristics of a RS-FF.

4. Conclusions

We have succeeded in the fabrication of RS-flip flop (FF) circuits based on pseudo-CMOS inverters by integrating fully solution processed OTFT devices. In order to reduce the variation of transistor characteristics, we have employed new type of transistors consisting of six transistors. We have successfully demonstrated a RS-FF circuit in ambient with excellent input-output performance.

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