Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp878-879

Annealing Effect on Field-Effect Mobilities in Bottom-Contact Alkylated Dinaphthothienothiophene Transistors

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Abstract

Effect of post annealing on the current characteristics of alkylated dinaphthothienothiophen (DNTT) thin-film transistors (TFTs) has been investigated. The annealing at 80 °C for long time dramatically improved the field-effect mobilities of the TFTs. The mobility of 3.3 cm^2/Vs was obtained in a bottom-contact alkylated DTNTT TFT.

1. Introduction

Organic materials having a potential for providing high mobilities of about 10 cm^2/Vs have been reported [1-6]. Alkylated dinaphthothienothiophene (Cn-DNTT) is one of the promising materials for high mobility p-channel organic thin-film transistors (TFTs) [1]. However, such high mobility demonstrated in long-channel transistors having top-contact configuration. On the other hand, short-channel organic transistors are demanded for the high frequency operation. Short-channel organic transistors are easily fabricated by adopting bottom-contact configuration. However, contact resistance between a contact electrode and a channel material limits mobilities in short-channel transistors.

We have demonstrated bottom-contact pentacene TFTs operating at high frequencies above 10 MHz [7]. Gold/AuNi drain/source electrodes modified with pentafluorobenzenethiol (PFBT), which are effective to reduce contact resistance, were used to realize the short-channel, high-mobility pentacene TFTs [8]. The modified electrodes are effective for C_{10}-DNTT TFTs as well as pentacene TFTs [9]. The mobility of 2.6 cm^2/Vs was obtained in the TFT with a channel length of 10 µm at an operational voltage of -15 V.

In this work, we report bottom-contact C_{10}-DNTT TFTs with contact electrodes modified with various benzenethiol derivatives. Effect of post annealing on the current characteristics of the TFTs is examined. The current characteristics of the TFTs with different-modified electrodes are compared, and are discussed on the basis of the contact resistance.

2. Experimental

Figure 1 shows cross-section of the C_{10}-DNTT TFT fabricated in this work. The chemical structure of C_{10}-DNTT is shown in the inset in Fig. 1. A silicon substrate with a 35-nm-thick SiO_2 layer was used as a substrate of the TFT. The SiO_2 has a unit area capacitance of 92.3 nF/cm^2. Drain/source electrodes of Au/AuNi modified with PFBT, 4-nitrobezenthiol (NBT), and 4-methylbenzenethiol (MBT) were adopted. Also, the TFT with unmodified electrodes was fabricated for comparison. The contact electrodes were patterned by photolithography and lift-off. The SiO_2 surface was treated with hexamethyldisilazane. C_{10}-DNTT was deposited through a metal mask. The substrate temperature was gradually increased from room temperature to 140 °C when depositing C_{10}-DNTT. The channel width (W) was 1 mm and the channel length (L) was in the range of 4 to 40 µm. Some TFTs were post-annealed in a dry-nitrogen glovebox at 60, 80, 100, and 120 °C. The current-voltage characteristic was measured in the glove box.

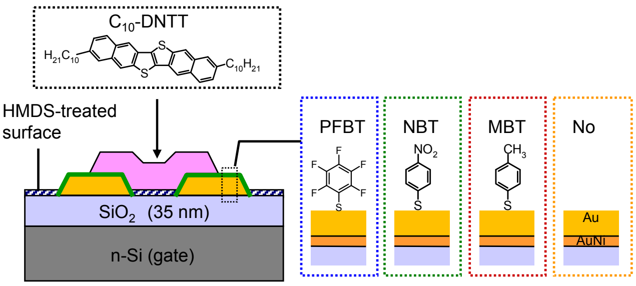

Fig. 1 Cross-section of a bottom-contact C_{10}-DNTT TFT.

3. Results

Figure 2 shows the drain current (I_D) versus gate voltage (V_G) characteristics of C_{10}-DNTT TFTs with contact electrodes modified with MBT. The characteristics shows the results measured for the TFT as-fabricated and annealed at 60, 80, 100, and 120 °C for 1 hour. The annealing in the range of 60 to 100 °C improved the current characteristics.

However, the annealing at 120 °C leaded to degradation of the current characteristics.

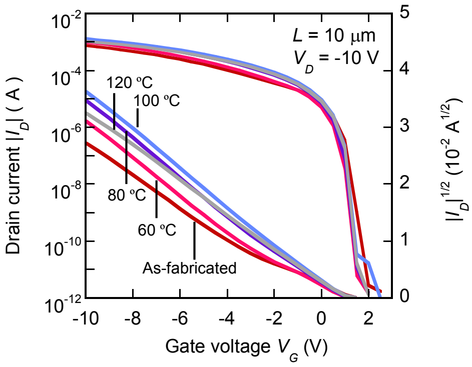

Fig. 2 Transfer characteristics of C_{10}-DNTT TFTs as-fabricated and annealed at 60, 80, 100, and 120 °C for 1 hour.

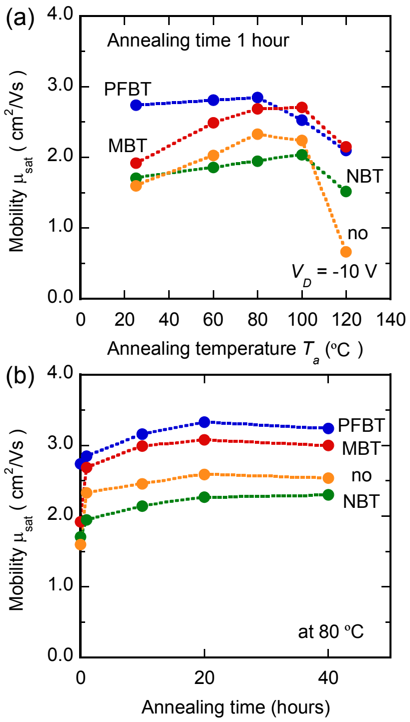

Fig. 3 (a) Annealing-temperature and (b) annealing-time dependence of mobilities in the saturation regime of C_{10}-DNTT TFTs.

The mobilities in the saturation regime (μ_{sat}) of C_{10}-DNTT TFTs with different electrode types are summarized in Figs. 3(a) and 3(b). The values were estimated by fitting a line to the $|I_D|^{1/2}$-V_G curve at a drain voltage (V_D) of -10 V. The annealing at 60, 80 and 100 °C for 1 hour improves the mobilities except for the TFT for PFBT. On the other hand, the annealing at 120 for 1 hour decreases the mobility. For 80 °C, the mobilities increase with the annealing time. For 20-hours-annealing, the mobilities of the TFTs with PFBT-, MBT-, NBT-modified and unmodified electrodes are 3.3, 3.1, 2.3, and 2.6 cm^2/Vs. Although the maximum mobility of 3.3 m^2/Vs was obtained in the TFT with PFBT-modified electrodes, the mobility of 3.1 cm^2/Vs for MBT is close to that for PFBT.

We estimated the contact resistance of the TFTs to discuss the change of the mobility. Figure 4 shows the normalized contact resistance (R_C W) of the TFTs as-fabricated and annealed at 60, 80, 100, and 120 °C for 1 hour. For instance, the R_C W value for MBT decreases with increase of the annealing temperature except that for 120 °C. The change of the contact resistances in Fig. 4 is consistent with the change of the mobilities. Thus, the change of the mobilities is mainly attributed to the change of the contact resistance caused by the annealing.

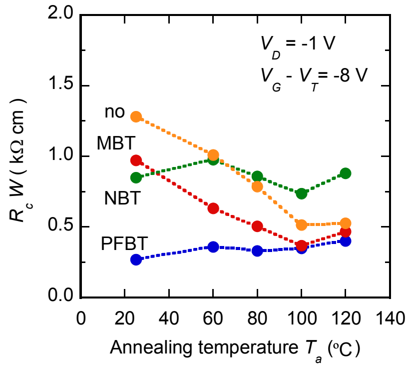

Fig. 4 Normalized contact resistances of C_{10}-DNTT TFTs as-fabricated and annealed at 60, 80, 100, and 120 °C for 1 hour.

4. Conclusions

We investigated the effect of post annealing on the current characteristics of bottom-contact C_{10}-DNTT TFTs with different electrode types. The annealing at temperatures less than 100 °C improves the current characteristics and the mobility. The change of the current characteristics is mainly attributed to the change of contact resistance caused by annealing. As a result, the mobility of 3.3 cm^2/Vs was obtained in the bottom-contact C_{10}-DNTT TFTs with PFBT-modified electrode.

Acknowledgements

This work was supported by Project for Developing Innovation Systems, MEXT and Grant-in-Aid for Scientific Research (C), Grand Number 24550211, JSPS. The authors would like to thank Nippon Kayaku Co., Ltd. for supplying us C_{10}-DNTT.

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