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Time Difference Amplifier and Its Application for TDC

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***Abstract*— This paper demonstrates a TDA, whose input time difference is amplified into the output time difference. Cross coupled chains of variable delay cells with the same number of stages are applicable for TDA, and the gain is adjusted via DLL-like closed-loop control. The TDA was fabricated using 65nm CMOS and the measurement results shows that the time difference gain is 4.78 at a nominal power supply while the designed gain is 4.0. The gain is stable enough to be less than 1.4% gain shift under ± 10% power supply voltage fluctuation. Applications of TDA for TDC is also discussed.**

I. Introduction

As the process technology advances, power supply voltage scales down while transistor switching speed increases. We are facing a new paradigm that time-domain resolution of a digital signal edge transition is superior to voltage-domain resolution of analog signal[1]. In this regime, time difference amplifiers (TDA) are the first to be required for time-domain operation, as well as time to digital converters (TDC) which is a front end block to convert a time-domain "analog" signal into a time-domain "digital" signal.

The concept of TDA, the input time difference is amplified at the output time difference as shown in Fig.1, was introduced[2] and utilized for TDC[3][4]. However, their TDAs use meta-stability of SR latch whose SET and RESET inputs have almost same rising time, and the recovering time from the meta-stability is approximately proportional to the input time difference. In addition to the meta-stability, they add delay T_{off} to the SET and RESET terminals to shift the meta-stability points to realize the time difference amplifier. The gain is expressed as $A_T = 2C/(g_m T_{off})$, which is decided by a transistor g_m and a load capacitor C. However, it is kind of "open-loop" gain, so their gain is easy to fluctuate by PVT variations.

This paper demonstrates a time difference amplifier whose gain is controlled by "closed-loop" so that the gain is stable against PVT variations[5][6].

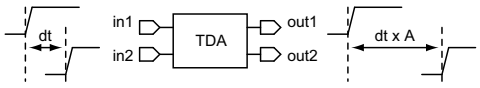

Fig. 1. Concept of time difference amplifier.

II. Circuit Design

The basic idea of our TDA is illustrated in Fig.2. A delay of a variable delay cell, shown in Fig.2(b), changes in accordance with a delay switch, and two chains of the delay cells are cross coupled as shown in Fig.2(a). In our example, the delay is 4:1 when the delay switch is H:L, and when the rising time

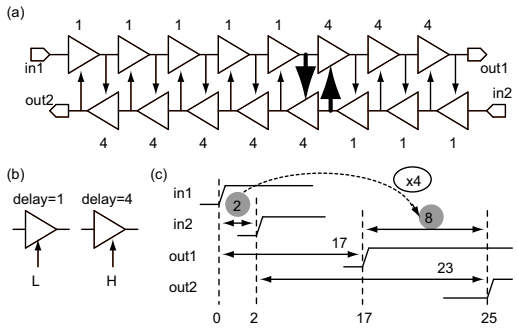

Fig. 2. Basic idea of our TDA. (a):Cross coupled chains of variable delay cells, (b):Variable delay cell, (c):Timing diagram.

difference for the input of the cross coupled chains *in*1 and *in*2 is 2, those signals propagate along the chains with the delay of each delay cell is 1 before the signals cross each other and then, the delay of each variable delay cell becomes 4. As shown in Fig.2(c), the delay time difference of *in*1 and *in*2 (2) is amplified in the delay time difference of *out*1 and *out*2 (8), here the gain, 4, is the delay ratio of the variable delay cell with its delay switch is H and L.

Figure 3 shows a block diagram of our TDA. The lower block adjusts the delay ratio of the variable delay cell with its delay switch of H/L to be 4. One chain has two delay cells with its delay switch is H, and the other chain has eight delay cells with its delay switch is L. The phase-frequency detector (PFD) detects the arrival time difference and the charge pump (CP) injects a charge to adjust the control voltage V_{ctrl} so as to match the delays of the two chains. When this DLL-like closed-loop locks, the delay ratio of the variable delay cell with its delay switch H/L is adjusted to be 4, and this V_{ctrl} is copied to the cross coupled chains of the upper block.

A schematic of the unit variable delay cell is shown in Fig.4. The control voltage V_{ctrl} is applied to the NMOS control *nctrl*,

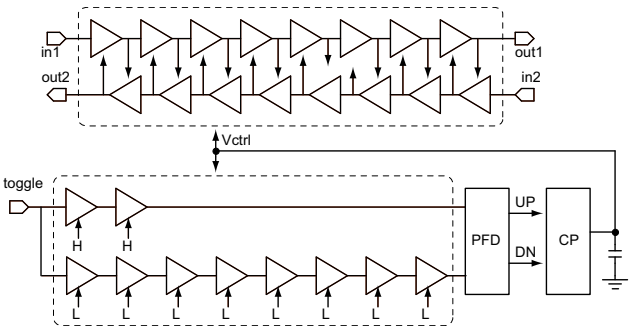

Fig. 3. Our TDA using DLL-like closed-loop control.

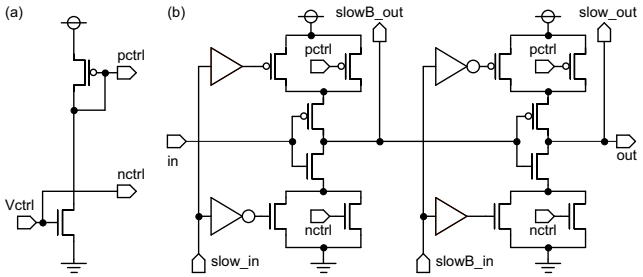

Fig. 4. Schematic of (a):Current mirror, and (b):Variable delay cell.

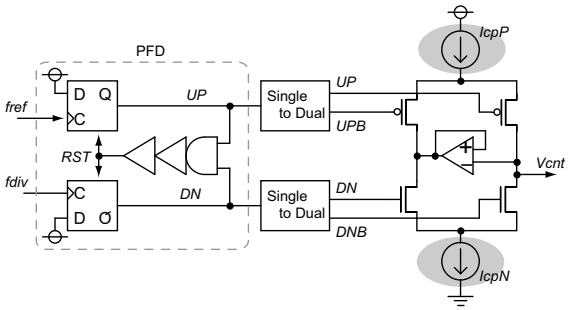

Fig. 6. PFD and CP.

and *pctrl* is generated by a current mirror shown in Fig.4(a). Lower V_{ctrl} makes wider delay difference of *slow_in* = H/L. All the variable delay cells share one current mirror circuit. *slow_in* is the delay switch and *slow_out* is connected to the delay switch of the other side of the delay chains. *slow_inB* and *slow_outB* signals are omitted in the previous figures for simplicity.

III. Measurement Results

Our TDA was designed and fabricated using 65nm standard CMOS technology. The core size is about 230μm × 490μm. The chip was measured by on-wafer probing. A pulse pattern generator outputs the signals for *in*1 and *in*2 with sweeping the delay of *in*2. The output signal of *out*1 and *out*2 are measured by a sampling oscilloscope and the delay difference is extracted from the waveforms. The measured input and output time difference are plotted in Fig.5(a)(b)(c) with different x range. The input-output relation is fitted into $y = ax + b$ with the graph (b), and the gain is 4.784 at the nominal power supply voltage 1.2V, and only ±1.4% fluctuation under ±10% power supply fluctuation. The TDA keeps the linearity with the input range of ±300ps at 1.08V where the output time

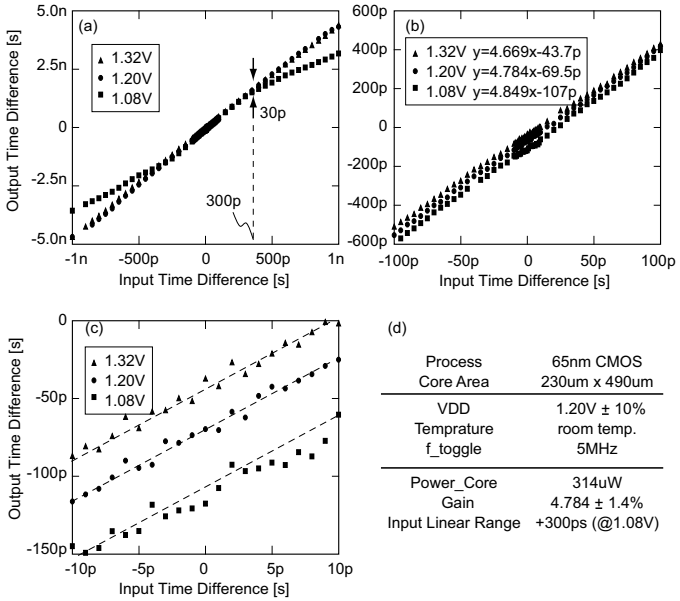

Fig. 5. (a)(b)(c):Measurement results of input time difference vs output time difference with three x-axis range, and (d):Table of the performance summary.

difference is about 30ps apart from the fitted line at 1.08V case as shown in graph (a). The power consumption of the core circuit is 314uW.

The reason that the gain is shifted from 4.0 is that the CP current source $I_{cp}P$ and $I_{cp}N$ shown in Fig.6 does not match because of the process variation, the two PFD inputs from the two chains of the delay cells, which is the lower block in Fig.3, does not match at the locked condition, resulting that the delay ratio of the variable delay cell with its delay switch of H/L bears away from the designed value.

The offset, the output time difference when the input time difference is zero, is caused by the pulse pattern generator delay offset and wire length difference of *in*1/*out*1 line and *in*2/*out*2 lines.

IV. Summary

We have demonstrated a TDA, whose input time difference is amplified into the output time difference. Cross coupled chains of variable delay cells with the same number of stages are applicable for TDA, and the gain is adjusted via DLL-like closed-loop control using PFD, CP and voltage controlled variable delay cells with their delay switch are H/L-fixed with different number of stages. Our proposed TDA was fabricated using 65nm CMOS and the measurement results shows that the time difference gain is 4.78 at a nominal power supply while the designed gain is 4.0. The gain is stable enough to be less than 1.4% gain shift under ± 10% power supply fluctuation.

V. Acknowledgement

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

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