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A Nano-Watt Power Rail-to-Rail CMOS Amplifier with Adaptive Biasing for Ultra-Low Power Analog LSIs

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Abstract

This paper presents a rail-to-rail folded-cascode amplifier (AMP) with adaptive biasing circuits (ABCs). The circuit uses a nano-ampere current reference to achieve ultra-low power and the ABC to achieve high speed operation. The ABC is based on the conventional one and modified to be suitable for rail-to-rail operation. Measurement results demonstrated that the AMP with the ABCs achieves high-speed, low-power, and stable operation in a wide input range of V_{SS} to V_{DD}. The AMP dissipated 352 nA when input voltage was 0.9 V.

1. Introduction

The demands for ultra-low power analog circuit design have been driven by next-generation energy-constraint applications. Analog front-end circuits for these devices are composed of active circuits using amplifiers (AMPs). Therefore, low power and high performance AMPs are strongly required.

An adaptive biasing circuit (ABC) is a well-known circuit to enhance speed of the AMP by using an adaptive bias current [1-5]. The ABC can provide low power and high speed operation. Most AMPs employing the ABC are designed with a low-gain wide-swing current mirror based AMP because they are easy to design thanks to its simple configuration. However, they cannot achieve higher gain. Moreover, the conventional ABC cannot be used for other types of high-gain amplifiers.

In this paper, we develop an ABC that solve the limitation in conventional ABC and propose a rail-to-rail folded-cascode AMP with the ABCs.

2. Issue of conventional ABC

In this section, we briefly summarize the operation of the conventional ABC [5] and explain the issue.

Figure 1 shows a schematic of the conventional ABC consisting of a differential pair (DP), a minimum current selector, and a current comparison circuit [5]. The DP detects potential difference between V_{IN1} and V_{IN2}, and converts them into currents I_1 and I_2. The minimum current selector, or two nMOSFETs connected in series, selects a smaller current I_{min} between them (I_{min} = min[I_1, I_2]). Control voltage of V_C is determined by the following equation.

$$I_{min} = 0.5I_B. \qquad (1)$$

When V_{IN1} = V_{IN2}, I_{min} is equal to $0.5I_B$ + $0.5I_{ADP}$ and thus I_{ADP} is not generated (I_{ADP} = 0). On the other hand, when

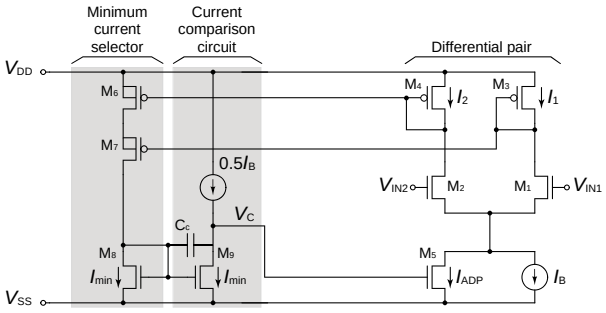


Fig. 1 Schematic of the conventional ABC [5].

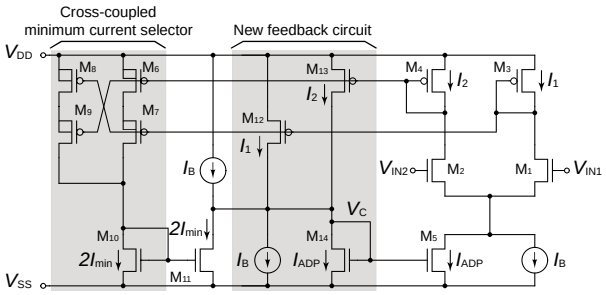


Fig. 2 Schematic of our proposed ABC.

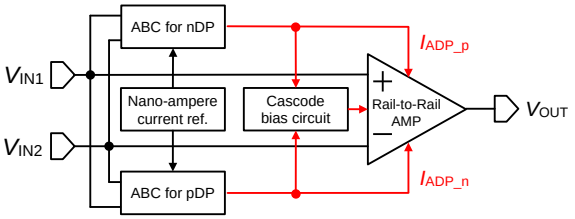


Fig. 3 Block diagram of our proposed rail-to-rail AMP.

$V_{IN1} \neq V_{IN2}$, I_{ADP} is generated because V_C increases due to the current reduction of I_{min} (= min[I_1, I_2]). In the subthreshold region, I_{ADP} can be expressed by using $|V_{IN1} - V_{IN2}|$ as

$$I_{ADP} = \frac{1}{2}\left\{\exp\left(\frac{|V_{IN1} - V_{IN2}|}{\eta V_T}\right) - 1\right\} I_B, \qquad (2)$$

where η is the subthreshold slope factor and V_T is the thermal voltage. Therefore, when the ABC detects the voltage change ($V_{IN1} \neq V_{IN2}$), it generates the I_{ADP} such that the AMP settles into the steady state condition (V_{IN1} = V_{IN2}) quickly.

The conventional ABC cannot be used in other high-gain AMPs (e.g., folded-cascode AMPs). The cascode voltages for such AMPs should be generated with the I_{ADP}. However, when the ABC accepts out of input voltage range of the DP, the DP enters into "dead zone". This makes V_C high, which is close to V_{DD}, and the V_C at this condition will generate abnormal large current in the bias circuit. The ABC cannot be used as it is. Therefore, we modify the ABC not to generate unwanted large current.

3. Proposed ABC and AMP

Figure 2 shows our proposed ABC. Two current paths consisting of M_{12}, M_{13}, M_{14}, and I_B are added in the conventional ABC. The control voltage V_C of the proposed ABC is determined according to the following equation,

$$2I_{min} = (I_1 + I_2) - I_{ADP}. \qquad (3)$$

When the DP is active, the ABC performs the same operation as the conventional one because both of $2I_{min}$ and $I_1 + I_2$ in Eq. (3) are equal to $I_B + I_{ADP}$ (see Eq. (1)). On the other hand, when the DP is dead, currents of I_{min}, I_{ADP}, and $I_1 + I_2$, become 0. This makes V_C low, which prevents large current generation. Thus, this circuit can stably operate over a wide input range of V_{SS} to V_{DD}. Note that, in our ABC, the minimum current selector is also modified to the cross-coupled circuit for a symmetric I_{min} generation.

Figure 3 shows the block diagram of our AMP. The AMP consists of a rail-to-rail folded-cascode AMP, a nano-ampere current reference circuit, a cascode bias circuit, and two ABCs for each n- and p-input DP.

4. Experimental Results

We fabricated a prototype chip of our proposed AMP (Prop.) using a 0.18-µm, 1P6M CMOS with deep n-well option. The conventional AMP (Conv.) [5] and AMP without adaptive biasing circuit (w/o ABC) were also fabricated in the same chip. Figure 4 shows a micrograph of the chip. The areas of Prop., Conv., and w/o ABC, were 0.0183 mm^2, 0.0168 mm^2 and 0.0072 mm^2. In the measurements, V_{DD} was set to 1.8 V. We used a commercial AMP as a buffer to drive the probe of the oscilloscope.

Figure 5 (a) shows the measured transfer curves. Prop. operated over wide input voltage range of 0 to 1.8 V, while Conv. operated within the limited input voltage of 0.3 to 1.5 V. Figure 5 (b) shows the measured current dissipation as a function of input voltage. Prop. dissipated 352 nA when the input voltage was 0.9 V. On the other hand, that of Conv. increased drastically at 0.3 and 1.5 V.

We measured the transient response of Prop. and Conv. with a unity-gain configuration. Figure 6 (a) and (b) shows the measured waveforms. The input frequency, peak-to-peak input voltage, and bias current, were set to 10 kHz, 1.5 V_{pp}, and 20 nA, respectively. Prop. showed the fastest speed, while Conv. could not operate correctly.

Table I summarizes measured and simulated performances. The slew rate in rising (SR+) of Prop. was three times faster than that of w/o ABC. Our proposed AMP achieved low power, high speed, and stable operation.

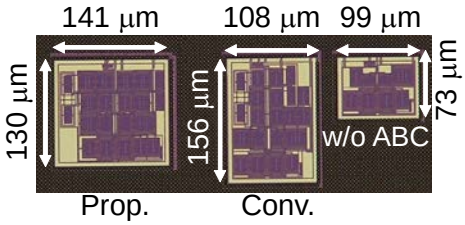


Fig. 4 Chip micrograph.

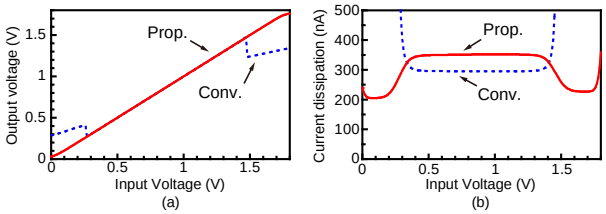
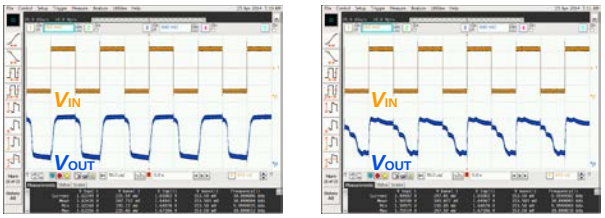


Fig. 5 Measured (a) transfer curves and (b) current dissipations as a function of input voltage.



(a) (b)

Fig. 6 Measured waveforms of (a) Prop. and (b) Conv. at 10 kHz, 1.5 V_{pp} input pulse.

Table I Performance summary of AMPs.

AMP		Prop.	Conv.	w/o ABC
Technology		0.18-µm CMOS		
Area (mm^2)		0.0183	0.0168	0.0072
Static current (I_B = 20 nA)	V_{IN} = 0.2 V	220 nA	224 µA	123 nA
	V_{IN} = 0.9 V	352 nA	295 nA	142 nA
	V_{IN} = 1.6 V	229 nA	116 µA	142 nA
SR (V/µs)* (@0.6 V_{pp}, 12.9 µW)	SR+	0.126	N/A	0.039
	SR-	0.067	N/A	0.052
SR (V/µs)* (@1.5 V_{pp}, 10.52 µW)	SR+	0.164	N/A	N/A
	SR-	0.249	N/A	N/A
DC Gain (dB)**		90.0	89.6	86.9
GBW (kHz)**		17.5	15.0	17.9
Phase margin (deg)**		88.8	89.1	92.3

*10 kHz input pulse **simulated value (C_L = 5 pF)

Acknowledgements

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