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Simulation, Fabrication and Initial Characterization of a Capacitive SiGe Integrated CMOS-MEMS High-G Accelerometer

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Abstract

This paper outlines the work done towards the conceptualization, simulation, fabrication and initial testing of a silicon-germanium (SiGe) integrated CMOS-MEMS high-G accelerometer for shock and impact sensing. Based on IMEC's SiGe MEMS platform, this sensor was developed to be more robust under high-G conditions while providing far better signal-to-noise ratio (SNR), lower power consumption and increased sensitivity when compared to other accelerometers with similar dynamic ranges. The MEMS offers a measuring range of ±5 kG and a bandwidth of 12 kHz. Chopper-stabilization technique was adopted for the low noise readout circuit of SiGe CMOS-MEMS microsystem. The CMOS readout circuit was implemented through the TSMC 0.18 μm process.

1. Introduction

CMOS-MEMS integration has emerged as a revolutionary concept today to vastly improve the performance of microsystems while allowing for smaller packages and lower instrumentation costs [1,2]. Majority of current MEMS still adopt the modular hybrid integration approach through means such as chip-to-wafer bonding, wafer-to-wafer bonding, etc [1,3,4]. However, this greatly increases the development time and costs for large volume manufacturing. In the case of accelerometers, several notable commercial examples such as the Analog Devices ADXL series use a monolithic approach but they only cater to low-G applications. In order to sense high-G, reliability of the sensor and package become cardinal. A monolithic integration scheme greatly increases accelerometer reliability at high-G ranges as it obviates the need for delicate interconnects. Furthermore, such an integration leads to better signal-to-noise ratio (SNR) through a reduced interconnect parasitic resistance and capacitance, faster response, lower power consumption and increased sensitivity - all playing a crucial role in improving performance while tracking and sensing high-G dynamic impact loads [1-3].

2. Device Characteristics

The device structure primarily consists of a centrally located proofmass suspended by support flexures and is 1.6 x 1.1 mm as shown in Fig. 3. A split comb-drive structure was employed for the sensing. IMEC's SiGe MEMS technology is based on a MEMS-last approach. The MEMS is processed on top of the CMOS readout circuits. Fig. 1 illustrates the cross-section of the process. This has proved to be the most promising means of integration as it enables independent optimization of the MEMS and CMOS to an extent. Also, new generations of CMOS can be appended to the structure without impacting the MEMS. The readout comprises of three essential building blocks – band-pass gain stage, synchronous demodulator and low-pass filter. The gain stage consists of a single ended amplifier, based on folded-cascode architecture, and helps to boost the SNR. It works within the frequency range 100 kHz–18 MHz, where the low corner frequency is determined by $1/2R_fC_f$ while the upper corner by the unity-gain bandwidth of the amplifier. Fully differential sinusoidal carriers excite the MEMS accelerometer and the output in response to the acceleration experienced is fed to the readout. The frequency of carriers is typically kept within 150 kHz–1 MHz to ensure that the results are obtained in the flat-band region. The amplified signal is then synchronously demodulated by envelope detection. This is followed by an on-chip 2nd order Sallen-Key low-pass filter that helps to remove the high frequency noise components. The cut-off frequency of low-pass filter is close to 200 Hz. This multilayer monolithic approach limits the thermal budget for processing the MEMS. Poly-SiGe meets material and reliability requirements for MEMS applications at significantly lower process temperatures than poly-Si making it best suited for MEMS-last integration [1].

Electromechanical Simulations

The MEMS, designed on *Coventor* was subjected to a series of electromechanical simulations to ensure linearity through fully differential sensing as well as optimize electrical response characteristics towards high-G loads as shown in Fig. 4. FEA simulations were conducted to ensure structural integrity in harsh conditions. Furthermore, Input noise characteristics of the ASIC were simulated for good SNR within the operational bandwidth. The ASIC supply voltage was 3.3 V with a power consumption of 3.368 mW.

The input referred noise of the ASIC was 41.51 nV/√Hz.

Die Level Characterization

Finally, die-level characterization in the form of C-V testing was done to observe the functioning of several device samples under a high voltage sweep simulating to a certain degree the MEMS performance under high-G conditions.

Figures and Tables

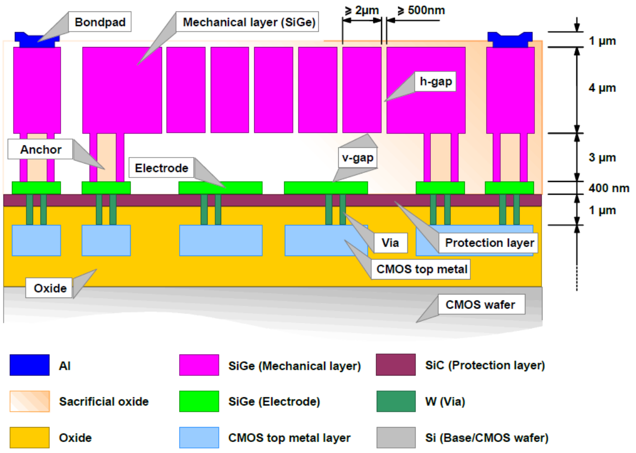

Fig. 1 Schematic of the SiGe MEMS process [2].

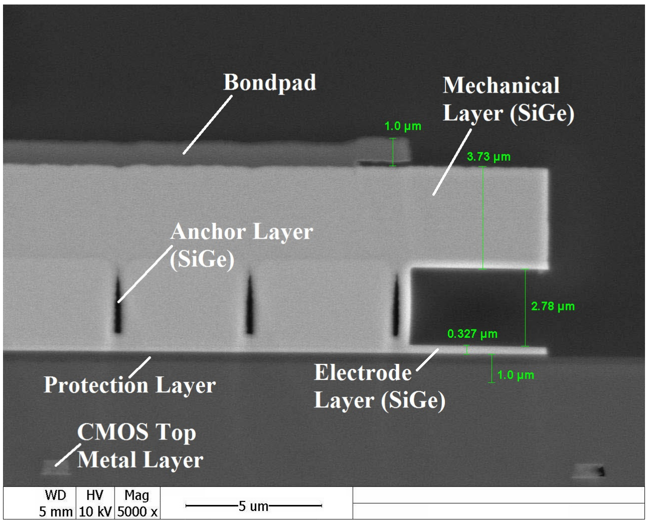

Fig. 2 SEM image of the accelerometer cross-section upon ion-milling.

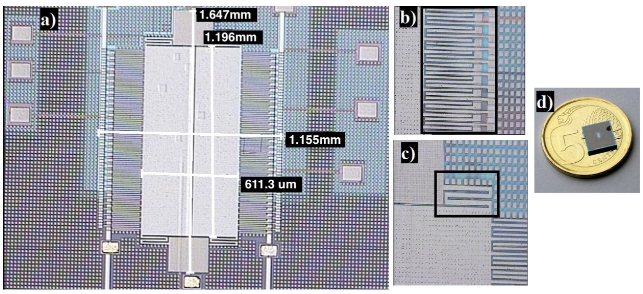

Fig. 3 a) Optical image of the MEMS, b) Split comb-drive structure (highlighted in black box), c) Support flexures (highlighted in black box) and d) Sensor die placed with a Singapore 5 cent coin.

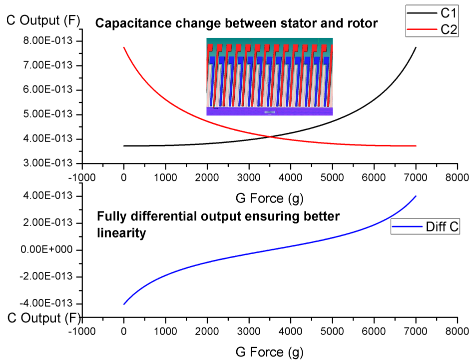

Fig. 4 Linear high-G dynamic electromechanical analysis of capacitance variation around the 5 kG dynamic range. Reduced nonlinearity obtained upon using differential sensing. Inset of split comb-drive shown.

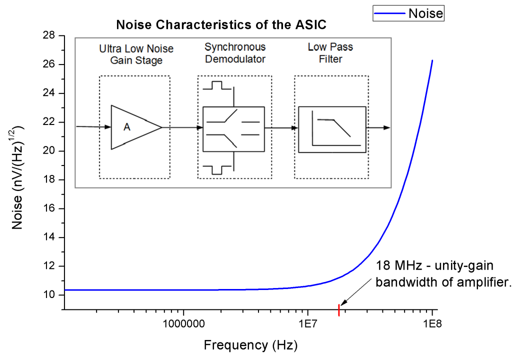

Fig. 5 ASIC input noise plot with an inset of ASIC block diagram.

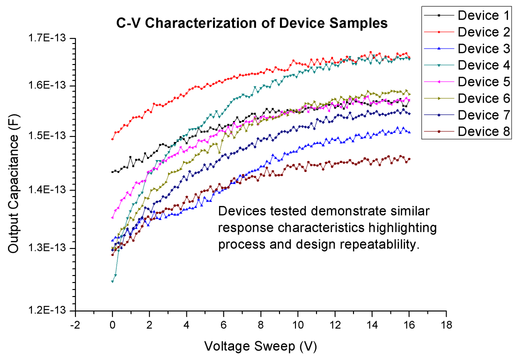

Fig. 6 C-V characterization of the CMOS-MEMS devices.

3. Conclusions

Overcoming design and process related challenges, an integrated CMOS-MEMS high-G accelerometer was successfully conceptualised and fabricated. Being one of the first of its kind, the sensor has been optimized to operate within the 5 kG dynamic range and is currently in the testing phase with a hermetically sealed packing underway.

References

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