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An RF Energy Harvesting Power Management Circuit with Timing Detection

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Abstract

This study presents an RF energy harvesting power management circuit for battery-less wireless sensor devices. The proposed circuit generates the power supply and activates main circuits at proper timing such as the beginning of communication. To detect the timing, the proposed circuit adopts an RF signal detector that reuses the RF energy harvester for the reduction of the input power loss and area. The fabricated circuit in 180-nm Si CMOS process demonstrates the RF signal detector senses the proper timing without the degradation of the charge efficiency. The total power consumption in charge phase achieves less than 124nW.

1. Introduction

RF energy harvester (RF-EH) enables battery-less operation of wireless sensor devices with little increase of device size. The recent studies have presented the RF-EH power management circuits that turn on the main circuits after RF-EH fully charges the storage capacitor [1, 2]. This type of the system can improve the sensitivity of RF-EH and extend the operation range. The reported system [1] turns on the receiver at the timing reaching the desired voltage in the storage capacitor, but the timing is uncertain because the timing depends on the strength of the RF signal. When the receiver activation timing is much earlier than the timing of transmission from reader, the communication establishment fails because the most of the energy in the storage capacitor is dissipated during the long waiting time. We propose the power management circuit that adopts an RF signal detector (RF-SD) as well as a sensor of the charged voltage. The proposed circuit can sense the proper timing such as the beginning of receiving or transmitting phase without degrading the charge efficiency.

2. System Overview

Fig. 1 shows the block diagram of the proposed power management circuit. The operation sequence is as follows that are corresponding to the timing diagram of Fig. 2(a).

① The RF-EH charges the storage capacitor by using the RF signal that comes from the reader.
② When the charged voltage (OUT_{EH}) reaches the desired voltage (V_U), the hysteresis comparator's output (EN_{CMP}) becomes high.
③ When the RF-SD senses the stop of the RF signal, the RF-SD's output (EN_{SD}) becomes high.
④ After both EN_{CMP} and EN_{SD} become high, the low dropout regulator (LDO) outputs the regulated voltage until OUT_{EH} decreases to the lower limit voltage (V_L).

The proposed circuit adopts not only the sensor of the charged voltage but also the RF-SD. The RF-SD senses the stop of the RF signal as the simple sign of the proper timing [2]. The timing diagram in Fig. 2(a) shows the deference between 'wi' (with RF-SD) and 'wo' (without RF-SD). By starting the communication at the proper timing, the receiver or transmitter eliminates the wasted activation time and energy use. Therefore, the stability of the communication establishment can be improved.

In this study, the hysteresis comparator sets V_U and V_L to 1.2V and 0.5V, and always monitors the charged voltage. The LDO provides 0.5V power supply, which aims to operate low power wireless transceiver, microcontroller.

3. Circuit Design

RF-SD

Fig. 3 shows the schematic of the proposed power management circuit. The RF-SD needs to sense the stop timing with the slight increase of the footprint and without the degradation of the charge efficiency. The proposed RF-SD reuses the 4th stage output (S4) of the RF-EH as the monitor terminal. By reusing a part of the RF-EH, the RF signal detection can be realized without the additional rectifier that causes the unnecessary footprint and power divide. In addition, the RF-SD shuts off the current until the storage capacitor is charged sufficiently to reduce drastically the power consumption in charge phase.

Fig. 2(b) shows the RF-SD operation in time domain. Until OUT_{EH} reaches V_U, EN_{CMP} is low state, and thus the N-MOSFETs (M1, M2) shut off the whole current consumption of the RF-SD under sub-nA. After exceeding V_U and while receiving the RF signal, EN_{CMP} becomes high state, and then, the current I_R flows through the resistor R1. At this time, I_R is supplied from the S4 output so that the voltage of S4 does not drop to below the threshold voltage of the inverter (V_{TH}). When stopping the RF signal, the S4 output cannot supply the current. The voltage of S4 becomes below the V_{TH}, and this is the detection of the stop of the RF signal.

RF-EH

To realize efficient charge in the storage capacitor, it is important to improve the RF to DC conversion efficiency. The RF-EH exploits a Dickson type charge pump circuit that uses the technique for threshold voltage compensation [3]. In the first six n-MOSFETs, their gate and backgate terminals connect latter stage output, which can provide the proper biased signal for the compensation. In addition, using the triple well process, the connections apply the forward body bias to the backgate terminals to lower the threshold voltage. The last two n-MOSFETs adopt diode connection to prevent the leak current through the

n-MOSFETs from the RF-EH output to R1.

4. Measurement Results

The proposed power management circuit was fabricated in a 180-nm Si CMOS process as shown in Fig. 4. Fig. 5 shows the output voltage of the RF-EH (OUT_{EH}) versus input power at 915MHz with 10MΩ load. The sensitivity of the RF-EH would be improved by using the impedance transformation circuit. Fig. 6 shows the power consumption in charge phase versus the charged voltage OUT_{EH}. The power consumption is less than 124nW and sufficiently lower than the RF input power level. Fig. 7 shows the RF signal (IN_{RF}), OUT_{EH} and OUT_{LDO} versus time at -3.6dBm input power using the 47-μF storage capacitor. The proposed system charges the storage capacitor with the RF signal and senses the the stop timing, and then the LDO outputs 0.5V.

5. Conclusions

The presented power management circuit generates the power supply by the RF-EH and contributes the stable wireless communication by detecting the proper activation timing.

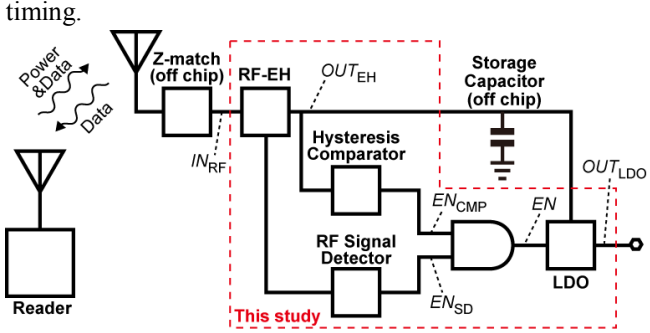

Fig. 1 Block diagram of the proposed power management system

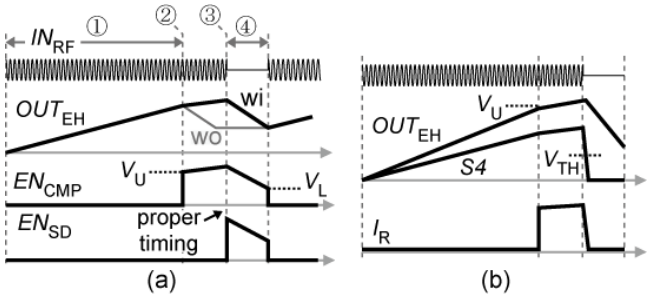

Fig. 2 (a) Timing diagram of the power management circuit
(b) Operation of RF-SD in time domain

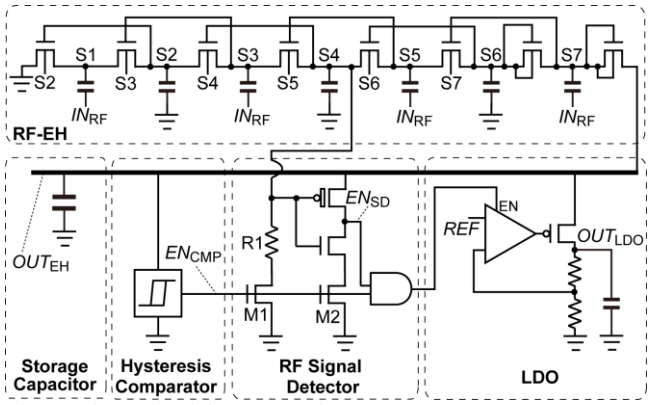

Fig. 3 Schematic of the proposed power management system

Acknowledgements

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References

[1] G. Papotto et al., IEEE J. Solid-State Circuits, vol. 49, no. 2, pp. 335–346, February 2014.

[2] U. Kaiser et al., IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 306–310, March 1995.

[3] G. Papotto et al., *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, September 2011.

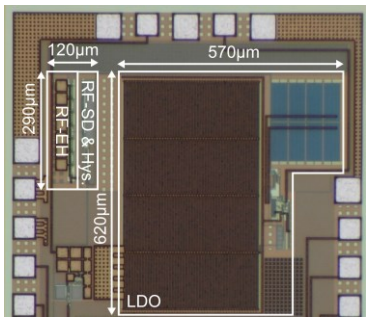

Fig. 4 Chip micrograph of fabricated circuit in Si CMOS 180nm

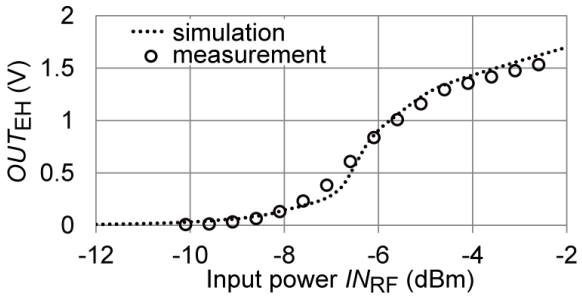

Fig. 5 Measurement and simulation results of OUT_{EH} versus input power IN_{RF} at 915MHz

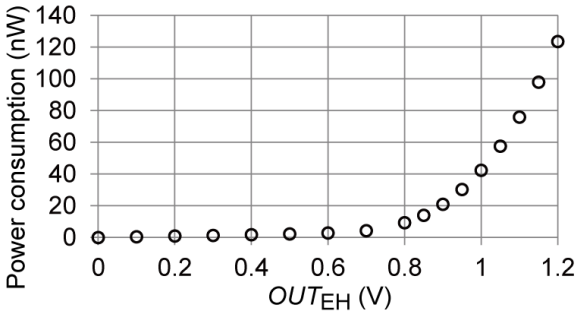

Fig. 6 Measurement results of power consumption versus OUT_{EH}

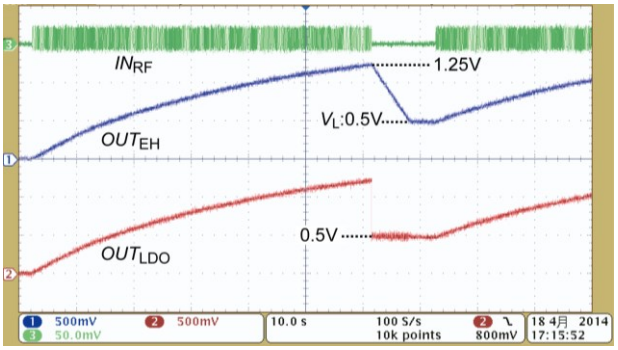

Fig. 7 Measurement results of IN_{RF}, OUT_{EH} and OUT_{LDO} versus time at -3.6dBm input power