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Improvement of Power Conversion Efficiency in Photovoltaic-Assisted UHF Rectifiers by Adopting Non-Silicide PV Cells

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Abstract

In the photovoltaic (PV)-assisted UHF rectifier, which is one example realization of the "synergistic ambient energy harvesting" concept, non-silicide PV cell structures were successfully adopted. Silicide blocking of PV cell area was experimentally verified to be effective for increasing photo-generated voltage, which resulted in the improved PCE of the rectifier by enhanced Vth compensation effect. 23.4% of PCE was achieved under conditions of an RF input power of -20 dBm, a frequency of 920 MHz, an output load of 47 kΩ, and a light illuminance of 221 lx. In addition, when the silicide blocking was applied to the voltage-boosted PV-cell structures, 31.2% of PCE was achieved at 2,770 lx.

1. Introduction

UHF rectifiers are attracting significant attention as a key component not only for wireless power transfer including RFIDs but also for the energy harvesting from ambient radio waves. In the UHF rectification, where the input signal amplitude is quite small, non-negligible turn-on voltage of rectification diodes, which is equal to Vth of MOSFETs in CMOS rectifiers, are the major cause of the rectification loss. Therefore, to increase the power conversion efficiency (PCE) by decreasing the loss, various Vth-compensation techniques have been proposed [1-3]. In [2], we have proposed a photovoltaic-assisted CMOS rectifier technology as one example of "synergistic ambient energy harvesting" concept, where Vths are compensated by bias voltages generated by photovoltaic (PV) cells (solar cells). Symmetric PV cell structures and voltage boost structures have been developed to increase PCE by balanced and increased photo-generated voltages [3]. However, different from the conventional solar power generation using PV cell, where output power can be increased by simply increasing PV cell area, the increase in photo-generated voltage by increasing area is difficult. In this study, we introduced a non-silicide PV cell structure, which was effective for increasing photo-generated voltage, and resultant increase in PCE of the rectifiers was demonstrated.

2. CMOS Rectifier Assisted by Non-Silicide PV-Cells

Fig. 1 shows a PV-assisted CMOS rectifier circuit with an equivalent circuit configuration of a PV cell. Two PV cells, each of which is composed of a simple pn junction diode, supply gate bias voltages to nMOS and pMOS separately. As shown in the equivalent circuit, a PV-cell under light irradiation can be modeled as a parallel connection of a diode and a current source. Since the PV cells are connected to gate electrodes of MOSFETs, they operate under open-circuit conditions and an output voltage is determined so as to equalize forward current of the diode with photo-generated current. Therefore, it is important to note that we cannot increase the output voltage of PV cells by increasing PV cell area since not only photo-generated current but also forward current increases for the same amount, resulting in the same forward voltage.

Silicide, a compound of metal and silicon, is widely utilized in today's integrated circuit technologies since it is indispensable to decrease contact and sheet resistances of

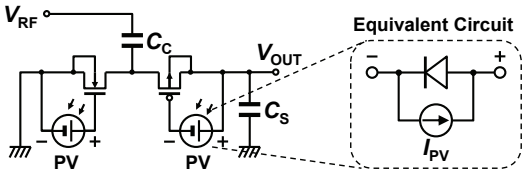

Fig. 1 PV-assisted CMOS rectifier circuit.

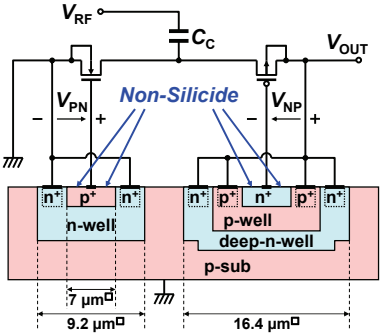

Fig. 2 CMOS rectifier with non-silicide PV cells.

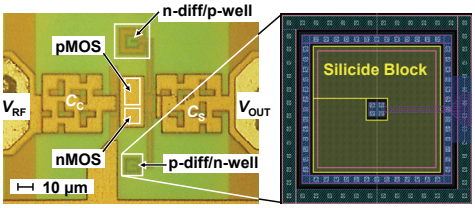

Fig. 3 Photomicrograph of the test circuit.

miniaturized semiconductor devices. Silicide film formed on a pn junction, however, degrades photo transmittance and possibly causes the increase in junction leakage current due to a stress-induced defects and metal impurity contamination. Therefore, in the CMOS imager technology, non-silicide photodiode is utilized to maintain sensitivity of pixels [4]. In this study, we applied the non-silicide technique to the PV-cells monolithically-integrated with the rectifier for increasing the output voltages.

Fig. 2 shows a CMOS rectifier with non-silicide PV cells. Symmetric PV cell structures realize balanced bias voltage generation. Almost all surface areas of principal junctions of PV cells, which are p^+-diffusion/n-well junction for nMOS bias voltage (V_{PN}) generation and n^+-diffusion/p-well junction for pMOS bias voltage (V_{NP}) generation, were prevented from silicidation. Contact areas were silicided due to constraint of the design rule.

3. Experimental Results and Discussions

Fig. 3 shows a photomicrograph of the fabricated rectifier test circuit with a layout sketch of a non-silicide PV cell. A 0.18-μm 5-ML CMOS process was used. The channel width and length of the nMOS were 3.6 μm and 0.18 μm, respectively, and those of the pMOS were 10.8 μm and 0.18 μm, respectively. The transistor area was covered by the top two metal layers for shading. Non-silicide PV cells were designed by covering principal junction areas with silicide block layer.

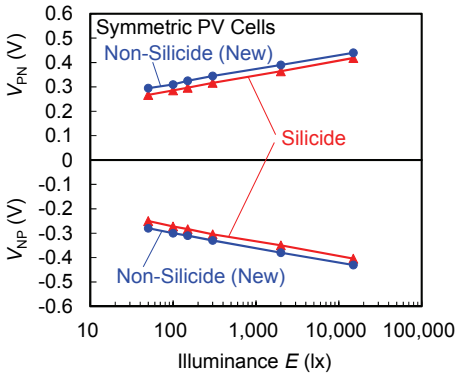

Fig. 4 Measured output voltages of PV cells.

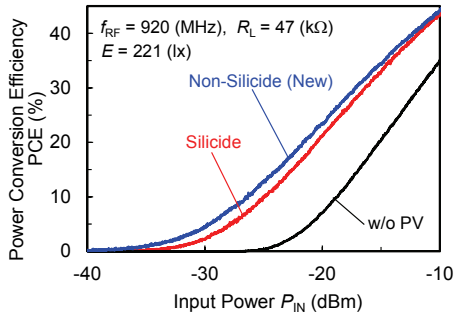

Fig. 5 Measured PCE as a function of P_{IN}.

Fig. 4 shows measured photo-generated output voltages of the PV cells. V_{PN} and V_{NP} were plotted as a function of illuminance E. A fluorescent light was used as the light source to emulate normal indoor environment. Illuminance level of typical indoor conditions are 100 lx to 1,000 lx. The newly-adopted non-silicide PV cells can generate 0.025~0.03 V larger bias voltages than the previous silicide PV-cells under the entire range of illuminance.

PCE of the rectifier was then evaluated. Measurements were performed at an RF input frequency of 920 MHz and an output load resistance of 47 kΩ. A vector network analyzer was used to apply RF power to the rectifier and to measure a reflection coefficient, S11. Input power P_{IN} was calculated using measured S11.

In Fig. 5, measured PCE under the illuminance level of 221 lx was plotted as a function of P_{IN}. 23.4% of PCE was achieved at a -20 dBm input by the newly developed rectifier with non-silicide PV cells, which corresponds to a 10% relative increase as compared with the previous silicide PV cells and is 3.3 times larger than the conventional rectifier without PV assistance.

Improved performance was more clearly shown in Fig. 6, where PCE dependence on the illuminance is plotted. Within the entire illuminance level of indoor lighting, the rectifier with non-silicide PV cells has superior PCEs. However, PCE has a saturation tendency at higher illuminance levels. It is caused by increased loss due to excess bias voltages.

Non-silicide PV cell technique was also applied to the rectifier equipped with the voltage-boosted PV-cells as shown in Fig. 7. For nMOS biasing, a deep n-well was added to increase quantum efficiency by acting as a diffusion barrier for photo-generated holes. For pMOS biasing, a hybrid PV-cell structure was introduced, where a junction for photo carrier generation and a dummy junction for photo carrier compensation were separated. The balance between nMOS and pMOS biasing voltages gets even

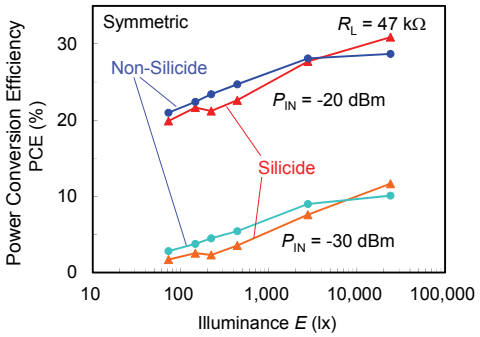

Fig. 6 Measured PCE as a function of illuminance.

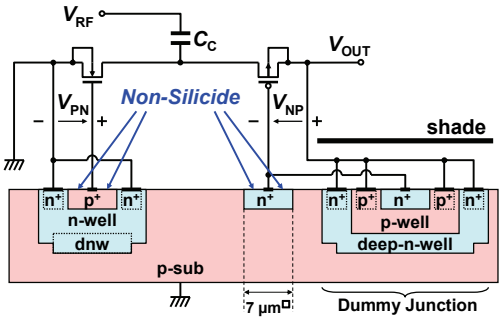

Fig. 7 Rectifier with voltage-boost PV cells.

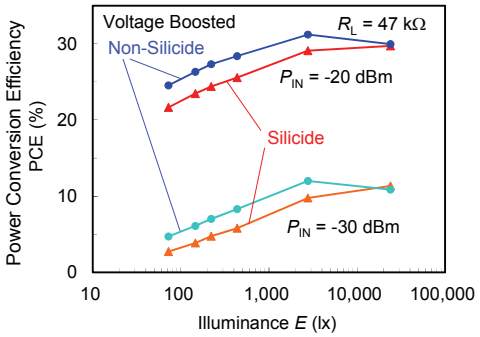

Fig. 8 Measured PCE.

worse but improved PCEs under low illuminance conditions can be expected. Measured PCEs are shown in Fig. 8. Although saturation tendency in large illuminance range became noticeable, the improvement in PCE by non-silicide PV cells are more significant under typical indoor lighting conditions. Peak PCE of 31.2% was achieved at the illuminance of 2,770 lx.

4. Conclusions

Non-silicide photo-diode technique has been successfully applied to monolithically integrated PV cells of the PV-assisted UHF rectifier for improving the efficiency. PCE of the rectifier were increased all over the typical indoor lighting conditions.

Acknowledgements

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