Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp984-985

# A 0.5-V 5.8-GHz Highly Linear VCO with Back-Gate Tuning Technique

Sho Ikeda, Sang_yeop Lee, Hiroyuki Ito, Noboru Ishihara, and Kazuya Masu

Tokyo Institute of Technology
4259-S2-14 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan
Phone: +81-45-924-5031 E-mail: paper@lsi.pi.titech.ac.jp

**Abstract**

**This paper proposes a VCO which achieves highly linear frequency tuning under a power supply of 0.5 V. To obtain the linear frequency tuning of a VCO, we focus on high linearity of the threshold voltage of a varactor versus its back-gate voltage. This enables linear capacitance tuning of the varactor, thus highly linear VCO can be achieved.**

**The proposed VCO was fabricated in 65 nm CMOS process. It shows the ratio of the maximum $K_{VCO}$ to the minimum one of 1.28. The dc power consumption is 0.33mW at a supply voltage of 0.5 V. The measured phase noise at 10-MHz offset is -123 dBc/Hz at the output frequency of 5.8-GHz.**

## 1. Introduction

To construct wireless sensor network, wireless sensor nodes with low power consumption are required to reduce the cost of battery exchanges. To reduce the power consumption of wireless sensor nodes, low supply voltage has become one effective approach, especially for digital circuit. However, the use of low supply voltage makes analog circuit design difficult because it would degrade maximum operation frequency, signal-to-noise ratio, and any other analog performances. One of the most difficult issues of low voltage analog is a voltage controlled oscillator (VCO) which is a key component in PLL which generates carrier signals in wireless systems, because it determines phase noise and power consumption. This paper focuses on the non-linearity of VCO. Lower supply voltage also means smaller active control voltage range of the VCO for frequency tuning. Therefore, to maintain certain frequency tuning range, frequency-voltage curve of the VCO is steep and the slope ($K_{VCO}$) varies severely in different control voltage region [1]. The non-linearity of the VCO may deteriorate the PLL stability and phase noise characteristics.

This paper proposes a highly linear VCO under the supply voltage of 0.5 V. Using back-gate of the pMOS varactor for frequency tuning improve the linearity of the VCO.

## 2. Proposed Back-Gate Tuning Technique

To achieve high linear VCO, high linearity of the varactor is necessary [2]. Numerous methods for linear frequency tuning of VCO have been proposed [1-3], however, these works cannot work effectively in the low voltage region because of the limited threshold voltage of MOS transistors. Linear function which can be used under low supply voltage is threshold voltage of MOS transistor versus its back-gate voltage. It is one of the few linear functions of MOS transistor which is non-linear elements. The threshold voltage of pMOS transistor is changed linearly when its back-gate voltage is swept as shown in Fig. 1. From other viewpoint, capacitance of the MOS also changed linearly.

Fig. 2 shows proposed VCO with back-gate tuning technique. To improve linearity, back-gate voltage of the pMOS varactor is used as control voltage for frequency tuning.

Among many types of VCOs, current-reuse topology is employed as a carrying vehicle of the proposed technique because it is the most effective one enabling low power operation with low phase noise. By using stacked structure of nMOS and pMOS as cross-coupled pair, same current from VDD is flowing into these nMOS and pMOS, which means the current is reused and reduced by half compared with conventional cross-coupled VCO. In addition, the current-reuse VCO can achieve lower phase noise characteristics compared with the conventional nMOS cross-coupled VCO because the flicker noise of pMOS is smaller.

## 3. Measurement Results

The proposed VCO was fabricated in a 65 nm CMOS process. Fig. 3 shows a chip micrograph of the proposed VCO. Its area is 630μm×640μm including testing pads. During the measurement, the supply voltage of 0.5 V was used for the VCO.

Fig. 4 shows measured output spectrum. The oscillation signal of 5.79GHz was observed.

Fig. 5 shows measured frequency tuning range. Control voltage means the back-gate voltage of the varactor. $K_{VCO}$ was calculated by using the 6th order approximation to remove the effect of noise on the measured frequency data. This figure shows that linear frequency tuning was achieved over all active control voltage range (0~0.5 V ). The maximum and minimum value of the $K_{VCO}$ was 37.3 MHz/V and 29.2MHz respectively, and its ratio is 1.28. This is equal to or greater than previous works [1-3] in spite of its low supply voltage.

Fig.6 shows measured phase noise characteristics when the output frequency was 5.78 GHz. The phase noise at 10-MHz offset was -123 dBc/Hz. The power consumption was 330μW under the supply voltage of 0.5 V. The proposed VCO achieved the figure of merit (*FOM*) of -183 dBc/Hz. The *FOM* is defined as

$$FOM = L(\Delta f) - 20\log(\frac{f_{\text{out}}}{\Delta f}) + 10\log(\frac{P_{\text{DC}}}{1\text{mW}})$$

where $L(\Delta f)$, $\Delta f$, $f_{out}$, and $P_{DC}$ are the phase noise, the offset frequency, the output frequency, and the power consumption respectively. It is similar value of *FOM* compared to previous works [1-3] in spite of its high linearity.

## 4. Conclusion

We proposed the highly linear VCO at a supply voltage of 0.5 V. Using back-gate voltages as control voltage for frequency tuning of VCO, linearity of the VCO can be improved. In addition, current-reuse topology of the VCO can achieve low power and low phase noise even in low supply voltage.

The concept was verified with a chip fabricated in 65 nm CMOS process. The ratio of the max $K_{VCO}$ to the minimum one of 1.28 and the *FOM* of -183 dBc/Hz was achieved. Proposed VCO can improve the PLL stability and phase noise characteristics under low supply voltage by its high linearity.

**Acknowledgements**

This work was partially supported by STARC, KAKENHI, and VDEC in collaboration with Agilent Technologies Japan, Ltd., Cadence Design Systems, Inc., and Mentor Graphics, Inc.

## References

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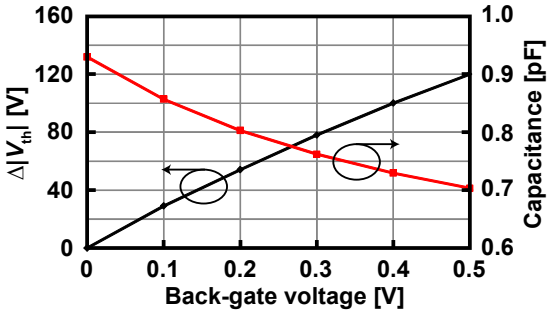


Fig. 1 Simulated capacitance and increment of threshold voltage of pMOS varactor versus back-gate voltage. ($V_{SG}$=$V_{SD}$=0.2V when the capacitance is simulated.)

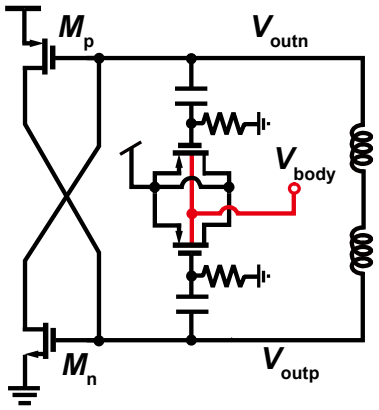


Fig. 2 Proposed VCO with back-gate tuning

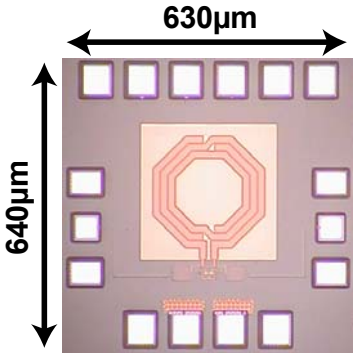


Fig. 3 Chip micrograph.

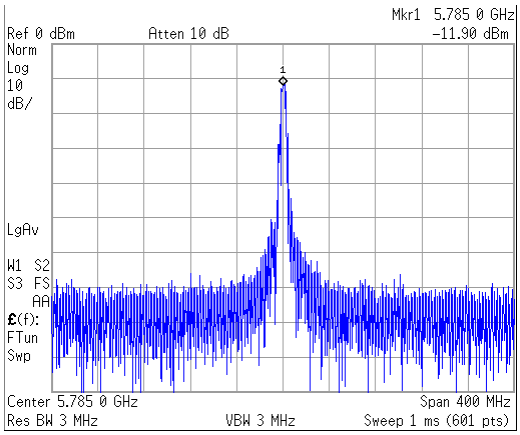


Fig. 4 Measured output spectrum at $f_{out}$ = 5.79GHz.

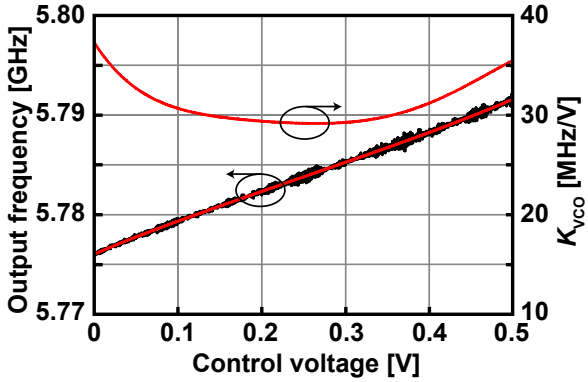


Fig. 5 Measured tuning range and VCO gain ($K_{VCO}$).

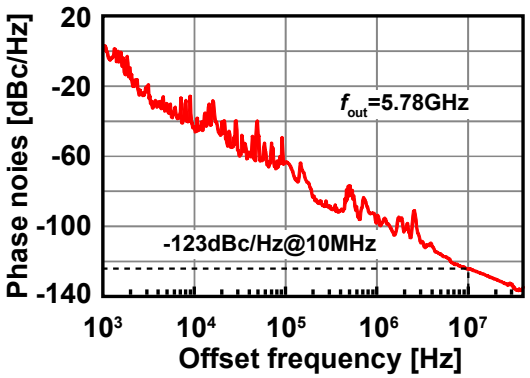


Fig. 6 Measured phase noise characteristics at $f_{out}$ = 5.8GHz.