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300 μs Short Interval Continuous Capturing Image Sensor with C-axis Aligned Crystalline Oxide Semiconductor FET/ p-channel Silicon FET Stacked CMOS Structure

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Abstract

Short interval continuous capturing is achieved by an image sensor whose pixels utilize c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO)-based FETs. CAAC-IGZO is a crystalline oxide semiconductor. The capturing method does not require A/D converters or other components to operate at high speed; therefore, it is applicable for an image sensor whose peripheral circuits utilize stacked CMOS circuits of CAAC-IGZO FETs and p-channel silicon FETs.

1. Introduction

Because of an extremely low off-state current of a c-axis aligned crystalline In-Ga-Zn-oxide-based FET (CAAC-IGZO FET) [1], various types of CAAC-IGZO FET-based LSIs [2-4] and an image sensor capable of an electronic global shutter [5] have been proposed. Note that CAAC-IGZO is a crystalline oxide semiconductor.

In this paper, an extremely short interval continuous capturing method for a CAAC-IGZO FET-based image sensor is proposed. The method enables continuous capturing at 300 μs intervals without brute-force A/D conversion, which requires a large-scale circuit and high power consumption as in conventional high-speed cameras. Furthermore, an image sensor with a stacked CMOS utilizing CAAC-IGZO FETs and p-channel Si FETs can also realize the proposed capturing method.

2. Short Interval Continuous Capturing

In a conventional high-speed camera, short-interval high-speed continuous image capturing is achieved by increasing the frame rate [6]. Thus, short time capturing/fast readout is required, which causes problems such as an increase in circuit area and an increase in the power consumption of A/D converters.

Figures 1 and 2 show a circuit diagram and a driving timing chart of pixels, respectively, for the proposed short-interval continuous capturing method. As shown in Figure 1, *n* pixels, each including four transistors, are connected to form one group by transistors that are connected to respective photodiodes (hereafter referred to as sharing transistors). Normal capturing of individual pixels can be performed by deactivating the sharing transistors. On the other hand, the proposed capturing can be performed by activating the sharing transistors and individually controlling transfer transistors in the pixels of the group by signal lines Tx1 to Txn though the resolution becomes 1/*n*. In Figure 2, pixels corresponding to the signal lines Tx1 to Txn are sequentially reset and exposed to light. After that, pixel data in the corresponding rows are sequentially read out, and the read data are converted into digital data by A/D converters.

As shown in Figure 3, in the proposed capturing method, continuous exposure can be divisionally performed at short intervals by dividing the selection time of the signal lines Tx1 to Txn and sequentially activating the signal lines Tx1 to Txn. After the continuous exposure, readout and A/D conversion of the captured data are sequentially performed. This implies that high-speed continuous capturing can be performed by short-time capturing/slow readout, and that A/D converters are not required to operate at extremely high speed. Thus, the proposed capturing method has advantages in circuit area and power consumption.

Although the period from exposure to readout varies depending on the pixel row, CAAC-IGZO FETs having an extremely low leakage current from nodes FD enable the proposed capturing method. Each of the nodes FD can be individually charged using the plurality of photodiodes that are connected through the sharing transistors. With such a structure, image degradation, because of shortened exposure time, can be reduced and the deviation of a captured image, because of position differences among the pixels, can be prevented.

3. Design and Measurement

To verify the proposed capturing method, we fabricated an image sensor utilizing CAAC-IGZO FETs for transfer transistors and sharing transistors in pixels and CMOS circuits of n- and p-channel Si FETs for peripheral circuits. The specifications of the image sensor are shown in the center column of Table 1. Figures 4 and 5 show a die photograph and a block diagram of the image sensor, respectively.

Images of an object rotating at approximately 6000 rpm are captured by the fabricated image sensor, and the captured images are shown in Figure 6. Note that the interval between the start of exposure Tx1 and the start of exposure Tx2 is set to 300 μs. Image (a) of the pixels corresponding to Tx1 and image (b) of the pixels corresponding to Tx2 show an approximately ten-degree rotation corresponding to 300 μs. In other words, it is confirmed that continuous capturing can be performed at short intervals by the proposed capturing method.

4. CAAC-IGZO FET/p-channel Si FET Stacked CMOS Image Sensor

The proposed capturing method does not require extremely high-speed operation for peripheral circuits and

other components. Further, the Vg–Id and noise characteristics of each of the FETs in stacked process of CAAC-IGZO FETs and n- and p-channel Si FETs shown in Figure 7 suggest that the driving ability increases as the size of the CAAC-IGZO FETs decreases and that CAAC-IGZO FETs tend to have an advantage over n-channel Si FETs with respect to noise. Thus, an image sensor whose pixels utilize CAAC-IGZO FETs and peripheral circuits, such as a driver and an A/D converter, utilize stacked CMOS circuits of CAAC-IGZO FETs and p-channel Si FETs can be expected to operate effectively. In other words, an image sensor without an n-channel Si FET can be expected to operate effectively. Thus, we fabricated the image sensor and confirmed whether its peripheral circuits can operate correctly.

The right column of Table 1 shows the specifications of the fabricated image sensor. The peripheral circuits utilize stacked CMOS circuits of CAAC-IGZO FETs and p-channel Si FETs. All the pixel transistors utilize CAAC-IGZO FETs. Figure 8 shows a pixel layout. The image sensor uses front side illumination and has a fill factor of 31%. However, if the image sensor uses back side illumination, the fill factor is 100%.

Figure 9 shows an example of the measurement results of the peripheral circuits. As shown in Figure 9, a column driver outputs an image data output enable signal (COUT) synchronized with a clock signal (CCK). From this result, it is confirmed that the peripheral circuits of the image sensor with a stacked CMOS of CAAC-IGZO FETs and p-channel Si FETs can actually operate.

5. Conclusion

Short interval continuous image capturing of CAAC-IGZO FET-based image sensor has been proposed. It has been demonstrated that short time capturing/slow readout can be achieved by the method though we need to quantify power consumption, analyze the relationship between the number of exposure divisions and sensitivity, and optimize portions using a stacked CMOS for precise analysis. Moreover, it has been examined that an image sensor including a stacked CMOS of CAAC-IGZO FETs and p-channel Si FETs is possible.

References

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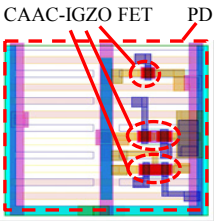


Fig. 8 Pixel layout of the stacked CMOS image sensor

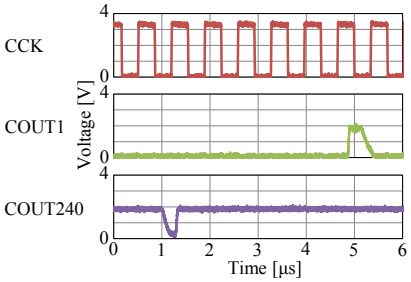


Fig. 9 Measurement waveforms of the column driver of the stacked CMOS image sensor

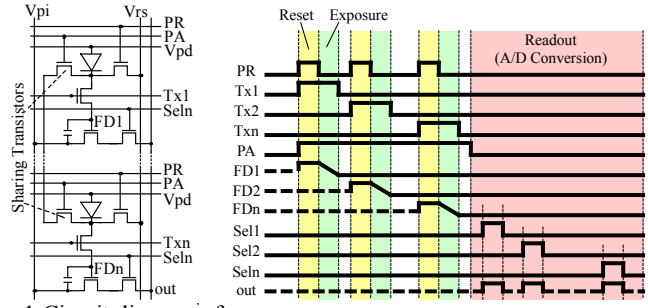


Fig. 1 Circuit diagram of group including pixels used for short interval continuous capturing

Fig. 2 Timing chart of short interval continuous capturing

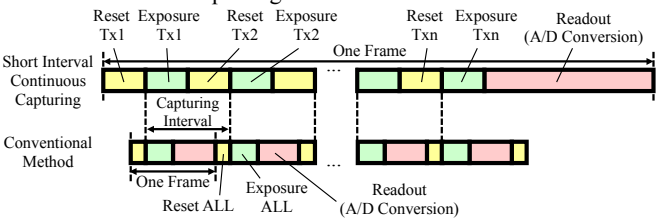


Fig. 3 Comparison between shutter methods

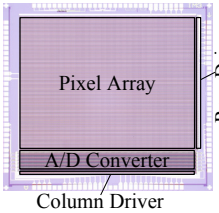


Fig. 4 Photograph of the CMOS image sensor

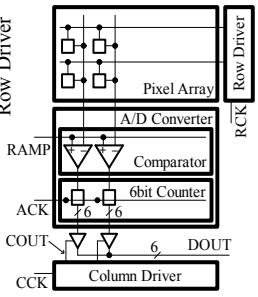
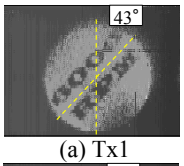
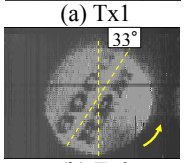


Fig. 5 Block diagram of the CMOS image sensor

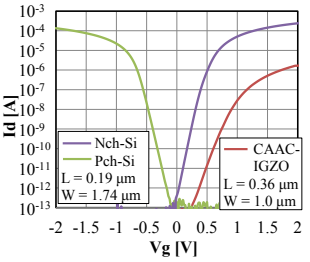


(a) Tx1

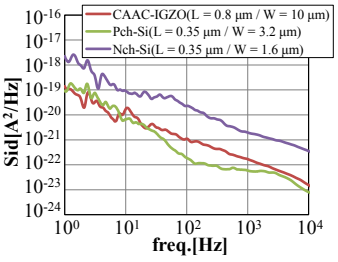


(b) Tx2

Fig. 6 Images obtained by short interval continuous capturing



(a) Vg-Id (Vd = 1.9V)



(b) 1/f noise

Fig. 7 Characteristics of FETs in stacked process of CAAC-IGZO FETs and n- and p-channel Si FETs

Table 1 Specifications of the fabricated image sensors

Technology Size	CMOS	Stacked CMOS
CAAC-IGZO FET	0.80 µm	0.35 µm
Nch-Si FET / Pch-Si FET	0.80 µm	0.18 µm
Die	CMOS	Stacked CMOS
Size	10.0 mm × 9.0 mm	6.5 mm × 6.0 mm
Pixel	CMOS	Stacked CMOS
Resolution	200 × 150	240 × 160
Size (1 pixel)	40 µm × 40 µm	20 µm × 20 µm
Fill Factor	15%	31 %
Exposure Division Number	2	2
A/D Converter	CMOS	Stacked CMOS
Type	Single Slope Integrating	Single Slope Integrating
Resolution	6bit	8bit
Voltage	3.3 V	1.8 V
Frequency (ACK)	528 kHz	3.53 MHz
Row Driver	CMOS	Stacked CMOS
Voltage	3.3 V	3.3 V
Frequency (RCK)	2.40 kHz	5.52 kHz
Column Driver	CMOS	Stacked CMOS
Voltage	3.3 V	3.3 V / 1.8 V
Frequency (CCK)	528 kHz	1.44 MHz