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A Platform for Backside Illuminated CMOS Image Sensors for UV and Visible Applications

B. Vereecke, C. Cavaco, K. De Munck, L. Haspeslagh,
K. Minoglou, D. Sabuncuoglu, K. Tack, and H. Osman
[1] imec, Kapeldreef 75, Leuven, B-3001, Belgium.
E-mail: bart.vereecke@imec.be

Abstract

Imec developed a platform for backside illuminated CMOS image sensors (CIS) that is adaptable for applications in the near ultraviolet (UV) region and visible range. Using HfO_2 as anti-reflective coating (ARC), a quantum efficiency (Q.E.) of more than 50% is reached for all wavelengths (λ) in the UV range from 260nm-400nm. In the visible region, Q.E. values between 75% and 90% are obtained for λ ranging from 400 to 700nm using Si_3N_4 as ARC coating. The process is developed on imec's 130nm Cu BEOL technology node and uses a monolithic approach where the photodiodes and read-out circuits are implemented on the same substrate. The substrate thickness is adaptable between 5μm and 30μm depending on the application and the design of the photodiodes.

1. Introduction

Over the last years, 200mm wafer process line at imec has been intensively used for the development, prototyping and low-volume manufacturing of highly specialized components in the sensors, MEMS and life-sciences areas. In this work we describe the platform for monolithic backside illuminated image sensors used in this facility for fabrication of high efficiency and specialized image sensors. The front side process part of the image sensors presented in this work is done in standard 130nm node CMOS fab at imec. However, backside processing part has also been applied to externally fabricated CIS wafers. We should note that some design considerations have to be taken into account to make the circuits compatible with the additional wafer-to-wafer bonding and backside processing steps that are specific to backside illuminated imager (BSI) manufacturing. This paper briefly describes this BSI processing steps for monolithic backside imagers, followed by an evaluation of the effect of BSI process part on the device performance in terms of dark current (D.C.) and quantum efficiency

2. Process Description

BSI process steps

The starting material for the BSI processing is a 200mm CMOS wafer with several back end of line (BEOL) copper metal levels but without final passivation and no bond pads on the front side (Fig. 1a). The CMOS substrate is a p+ boron-doped Si wafer with an 18um intrinsic EPI layer. The device wafer is then bonded to a silicon carrier wafer using oxide-oxide permanent bonding. After bonding the device wafer is thinned using a combination of grinding and Si wet etch (Fig. 1b). The target thickness after thinning can be chosen between 5 and 30μm depending on the application. After thinning the Si surface has to be passivated. Surface passivation is achieved by a shallow boron implant followed by a laser anneal step to activate the boron in the Si lattice[1]. The laser anneal results in a very local heating near the Si surface.

In the bond pad area of the die, a large Si trench is etched through the entire thickness of the device wafer (5-30um) to allow connection to the BEOL layers (Fig 1c). An anti-reflective coating is applied to improve transmittance of the incident light to the silicon diode. Inside the Si

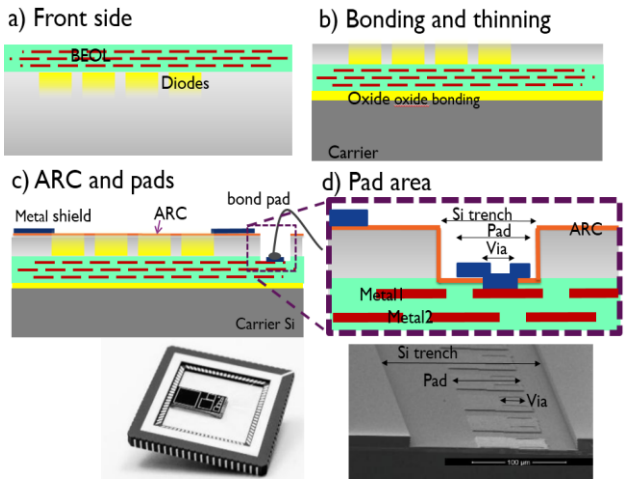

Fig. 1 Schematic of the BSI processing flow and actual pictures of packaged BSI and cross section SEM of the pad area.

trench some large vias are etched into the ARC layer and pre-metal dielectric layers, landing on the copper layer of the metal1 level in the CMOS process flow. A barrier and Aluminum layer are deposited as a bond pad material for wire bonding. These metals are then patterned to form the backside bond pads (similar to front side pads) and metal light shields on the diode periphery. Up to 5 metal levels of CMOS have been evaluated for the described BSI process.

ARC Layer Selection

Silicon nitride and hafnium oxide have been evaluated as ARC layers for Visible and near UV range, respectively. Since the ARC layer is exposed to the several wet strip steps and pad etch, the layers were evaluated for process compatibility with the via and pad patterning steps that are processed on top of the ARC.

Si_3N_4 is the material of choice for applications targeting

the visible spectrum (λ= 400-700nm). However, at shorter wavelengths the absorption of photons into the nitride increases and will reduce the transmittance of UV light to the device. HfO_2 is a material with very small absorption values in the UV region and is therefore better suited for applications targeting this part of the spectrum. Simulations showed that a HfO_2 layer of 25nm is well suited for a wide spectrum in UV region and a Si_3N_4 layer of 50nm is well suited for the visible light

3. Dark Current and Q.E. Measurements

Imec BSI process has been applied to several designs of image sensor arrays for various applications. For the evaluation of dark current and quantum efficiency a test device was used with large photodiodes 100µm*100µm up to 4500µm*4500µm. The large diodes are required to have sufficient sensitivity to measure the dark current directly and enhance the sensitivity of the Q.E. measurement.

Dark Current Measurements

The dark current is the intrinsic leakage current in the photodiode in reverse bias mode in perfectly dark conditions. This leakage current is a limit to the sensitivity of the diode to low-light conditions. In Fig. 2 wafer scale dark current measurements for various BSI process conditions (B-E) are compared to FSI wafers (A). The BSI and FSI

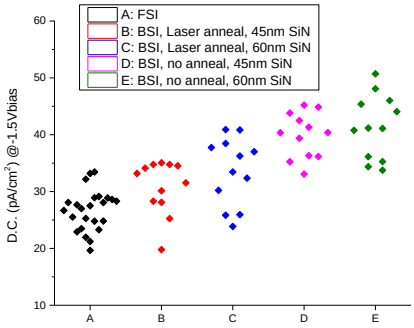

Fig. 2 Dark current measurement on FSI and BSI wafers

wafers went through the processing together for the front-end flow and the Cu metal layers. After top metal processing the FSI wafers were finished with standard passivation and front side bond pads, while the other wafers continued for the BSI flow, i.e. oxide-oxide bonding, thinning, etc. This ensures identical devices for all wafers for a direct comparison. The baseline of the front side wafer (A) is about 25pA/cm^2 at 25°C which is in the range of commercial BSI imagers [2]. The backside illuminated wafers show slightly higher values in the range to 25-50pA/cm^2. Samples without laser anneal tend to be a bit higher than annealed samples, although the effect is possibly within process variations.

Quantum Efficiency

The Q.E. of a photodiode is the efficiency at which the energy of the incident light is converted into electrical output energy. To achieve high Q.E. values, the incident light has to be absorbed in the active area of the photodiode. The reflection of light on the surface of the sensor is tuned by the ARC material, that is designed to minimize reflection and optimize transmittance to the silicon at a certain wavelength.

In figure 3 (top) the Q.E. measurements for various Si_3N_4 thicknesses are compared. The left shoulder on the peak shifts towards the lower wave lengths when reducing the nitride thickness. This behavior is as expected from transmittance simulations. The right side tail is also somewhat shifting but the reduction of Q.E. in this part of the spectrum is mainly limited by the Si thickness as longer wavelengths have longer absorption depth in Silicon, hence not related to the ARC layer. In the UV region (Fig. 3 bottom) the absorption coefficient of Si_3N_4 becomes too high

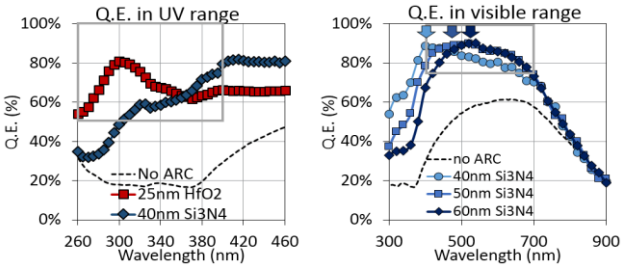

Fig. 3 Measured Q.E. on BSI photodiodes optimized for UV (top) and visible light (bottom)

for good Q.E. values and HfO_2 proves to be a better candidate. Up to 80% Q.E. is measured ~300nm wavelength for the HfO_2 thickness implemented. We have to note here that we have not observed any Q.E difference between laser annealed and non-laser annealed samples.

4. Conclusions

We evaluated the backside illuminated sensors produced in the imec 200mm silicon processing line. The platform is based on the 130nm Cu BEOL node technology in combination with 3D process technology for the BSI processing. Results show that with this BSI approach good dark current values of <50pA/cm^2 and Q.E. larger than 80% for visible and 50% for near UV were reached.

This baseline process is available and is being applied to fabricate various specialty imagers while further optimization of the process to accommodate different application needs is ongoing.

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