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Leakage-Delay Analysis of Monolithic 3D Logic Circuits using Ultra-Thin-Body InGaAs/Ge MOSFETs considering Interlayer Electrical Coupling

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Abstract— ***TCAD analysis results indicate that monolithic 3D inverter and 2-way NAND have better leakage and intrinsic delay performance with optimized interlayer electrical coupling for both ultra-thin-body (UTB) SOI and InGaAs/Ge devices compare with planar 2D structure. Besides, InGaAs/Ge devices exhibit larger improvement than SOI devices. The advantage of InGaAs/Ge devices increases with decreasing V_{DD}.***

1. Introduction

3D integration is promising to increase chip density and reduce interconnect delay. Among various 3D technologies, monolithic 3D integration, which stacks multiple layers sequentially facilitates ultra-fine inter-tier vias and short interconnection [1-2]. Moreover, monolithic 3D technology enables heterogeneous integration with various high-mobility channel devices. The implementation of two-tier monolithic 3D inverter using InGaAs/Ge devices has been successfully demonstrated [3]. With thin interlayer dielectric (ILD), the increasing electrical coupling may alter the characteristics of upper-tier devices, and offer the opportunity for optimization of monolithic 3D circuits [4-6]. In this work, we investigate monolithic 3D logic circuits with emphasis on the leakage and intrinsic delay considering interlayer coupling between layers based on physical layout to assess the potential of 3D integration using InGaAs/Ge UTB devices.

2. Monolithic 3D Structure and Simulation Methodology

For monolithic 3D structure, two-tier layer design, one for NMOSFET and the other for PMOSFET, is adopted and connected using dense nano-scale inter-tier vias (Fig. 1(a)). In our analysis, 3D logic circuits composed of InGaAs NMOSFET and Ge PMOSFET are investigated. Four possible scenarios with different materials (InGaAs/Ge and Si) and tier combinations ((Upper/Bottom) tier for (P/N) and (N/P) MOSFET) are shown in Fig. 1(b) for 3D logic circuits. For comparison, we use two back-gate biases (V_{bg} = 0V and V_{bg} = V_{DD} for NMOSFET and PMOSFET, respectively) for the evaluated 2D circuits and the bottom devices of 3D counterparts. With significant interlayer coupling, the gate of bottom-tier transistors serves as the V_{bg} of upper-tier devices.

In this work, TCAD mixed-mode simulations [7] are performed considering the interlayer coupling of monolithic 3D logic circuits. The calibrated SOI and InGaAs-OI/GeOI UTB devices [8] are with L_g = 25nm, T_{ch} = 5nm, EOT = 0.7nm, T_{BOX} = T_{ILD} = 10nm [9]. Designed with equal $I_{d,sat}$, Fig. 2 shows that the InGaAs-OI MOSFET, with higher mobility, possesses the highest $|V_T|$ whereas the SOI device has the lowest $|V_T|$. Besides, the GeOI devices have the highest I_{off} (due to band-to-band tunneling leakage, I_{BTBT}) at high drain bias, while the SOI counterpart shows the highest I_{off} (due to subthreshold leakage) at low drain bias. For delay analysis, fan-out 1 loading is considered with the input signal slew rate calculated from the multiple-stage inverter chains.

3. Results and Discussion

Fig. 3(a) shows the leakage comparison of 2D SOI and InGaAs/Ge inverter versus V_{DD} with input signal at "High" and "Low" ("0" and "1"). With significant I_{BTBT}, the InGaAs/Ge inverter exhibits slightly larger leakage than that in the SOI counterpart at high V_{DD} and "High" input signal. With decreasing V_{DD}, InGaAs/Ge inverter has lower leakage. In Fig. 3(b), monolithic 3D inverters stacked in (P/N) and (N/P) tier combinations are compared with the 2D counterparts. As can be seen, identical leakage is found due to the identical V_{bg} configuration of the monolithic 3D inverter through the leaky device to that in the 2D design [5].

Fig. 4 compares the delay improvements of various 3D 1-stage inverters over the 2D counterparts. Due to the strength enhancement of the upper-tier transistors, it can be seen that more than 10% improvement is achievable for the output falling and rising delays of (N/P) and (P/N) combinations, respectively. Moreover, the improvement becomes more significant at lower V_{DD} due to the enhanced back-gate bias efficiency at lower V_{DD}. Compared with SOI circuits, the InGaAs/Ge 3D inverters with larger back-gate bias efficiency exhibit higher performance enhancements over the 2D counterparts. Fig. 5 shows the delay advantages of various 3D SOI and InGaAs/Ge 5-stage inverters over the 2D cases. As can be seen, 3D SOI inverters stacked in (N/P) and (P/N) schemes have comparable delay improvement. For InGaAs/Ge 5-stage inverters, 3D design with (N/P) tier combination exhibits more enhancement over the (P/N) design and SOI counterparts, included the additional performance benefit using high-mobility channel devices in 3D inverters.

For monolithic 3D 2-way NAND, two possible designs depending on the alignment of input gate at different layer lead to direct and switched 3D layouts, as shown in Fig. 6. The comparisons of NAND leakage among various scenarios and input signals (A,B) are shown in Fig. 7(a) and (b) at V_{DD} = 1V. In Fig. 7(a), significantly larger leakages are found in 3D SOI 2-way NANDs with switched layout and (N/P) tier combination under (A,B) = (0,1) and (1,0). In such cases, the off-state NMOSFETs experience forward back-gate biases from the "High" input signal of the bottom-tier PMOSFETs, resulting in significant leakage increase. For InGaAs/Ge NANDs (Fig. 7(b)), lower leakage than the SOI counterparts are observed except for (A,B) = (1,1). The worst-case leakage, with input signal (A,B) = (0,1) and (N/P) tier combination, are shown in Fig. 8 across various V_{DD}. It is observed that 3D InGaAs/Ge NANDs exhibit lower leakage than that in the SOI counterparts except for the switched layout at high V_{DD}.

Fig. 9 compares the bottom switching delays for 2D/3D SOI and InGaAs/Ge NANDs. As can be seen, 3D NANDs stacked in (N/P) tier combination lead to more than 10% delay improvement due to the strength enhancement of the upper-tier transistors. Moreover, due to its significant back-gate bias efficiency, the benefit in InGaAs/Ge 3D NAND reaches 80% at lower V_{DD}.

Acknowledgment

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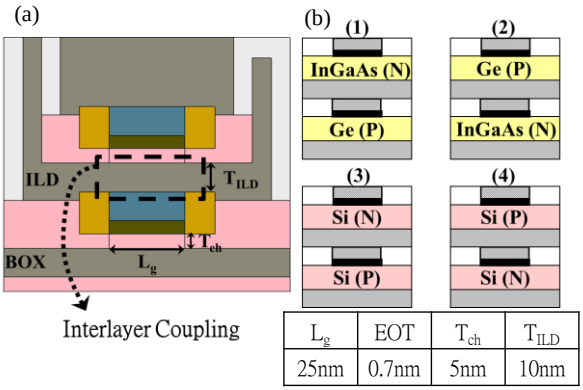

L_g	EOT	T_{ch}	T_{ILD}
25nm	0.7nm	5nm	10nm

Fig. 1. (a) Two-tier monolithic stacking showing the interlayer electrical coupling between tiers and, (b) the scenarios with different materials (InGaAs/Ge and Si) and various tier combinations evaluated in this work.

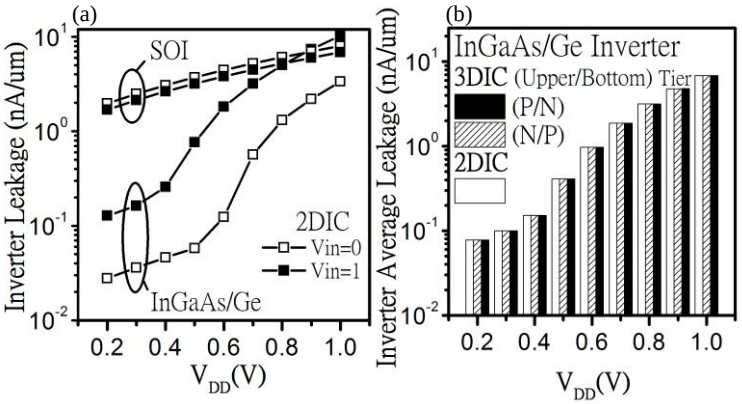

Fig. 3. (a) The leakage comparison of 2D SOI and InGaAs/Ge inverter at various V_{DD} with input signal equals to "High" and "Low" ("0" and "1"), and (b) the average leakage comparison of 2D and 3D ((Upper/Bottom) tier as (P/N) and (N/P)) InGaAs/Ge inverter versus V_{DD}.

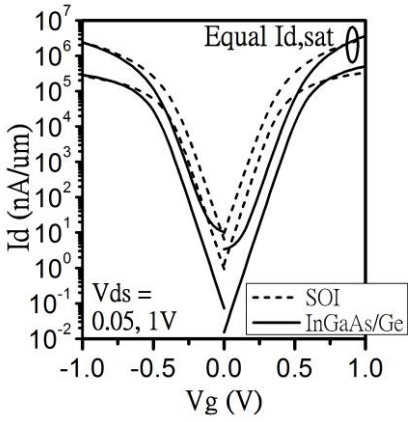

Fig. 2. The Id-Vg charateristics of CMOS with different materials (InGaAs-n/Ge-p and Si-n/Si-p) designed under equal Id,sat.

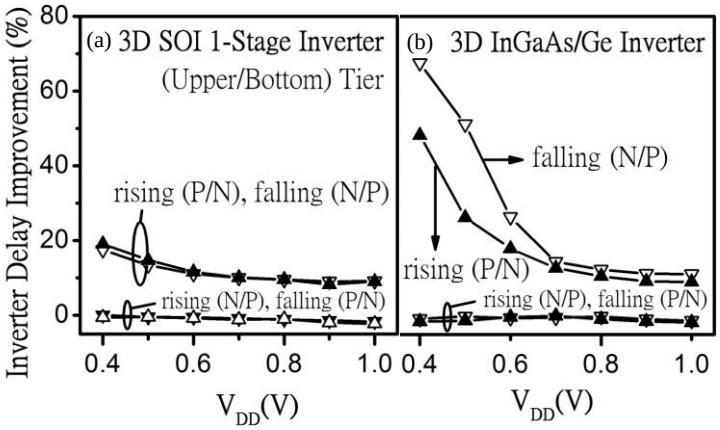

Fig. 4. The performance enhancement of (a) SOI and (b) InGaAs/Ge 3D 1-stage inverters over the 2D counterparts under various tier designs and V_{DD}.

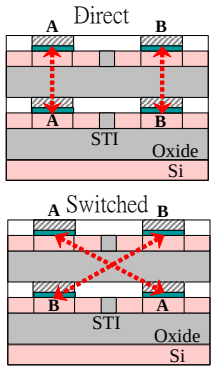

Fig. 6. Illustration of 3D 2-way NAND with direct and switched layouts.

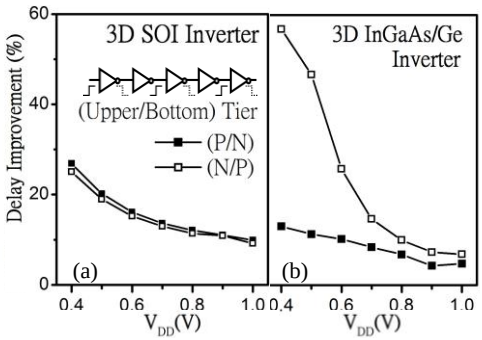

Fig. 5. The performance enhancement of (a) SOI and (b) InGaAs/Ge 3D 5-stage inverters over the 2D counterparts under various tier designs and V_{DD}.

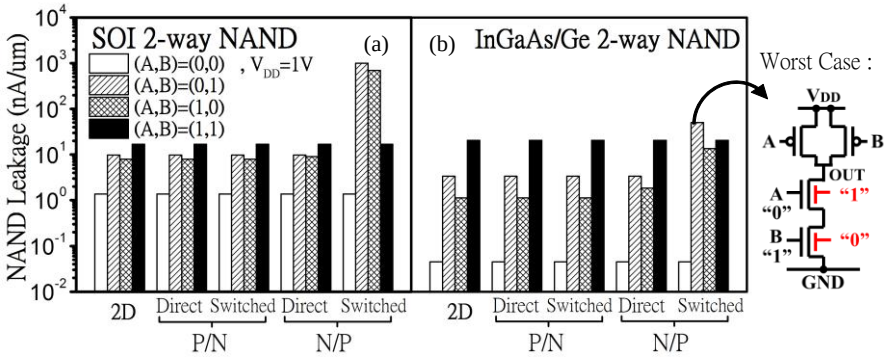

Fig. 7. Leakage comparison of (a) SOI and (b) InGaAs/Ge 2D/3D 2-way NANDs with various layout designs, tier combinations and input signals.

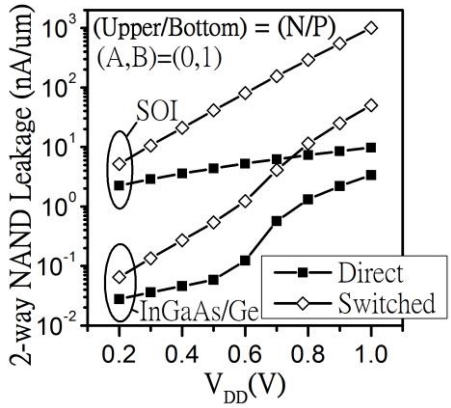

Fig. 8. The comparison of worst-case leakage for InGaAs/Ge and SOI 3D NANDs versus V_{DD}.

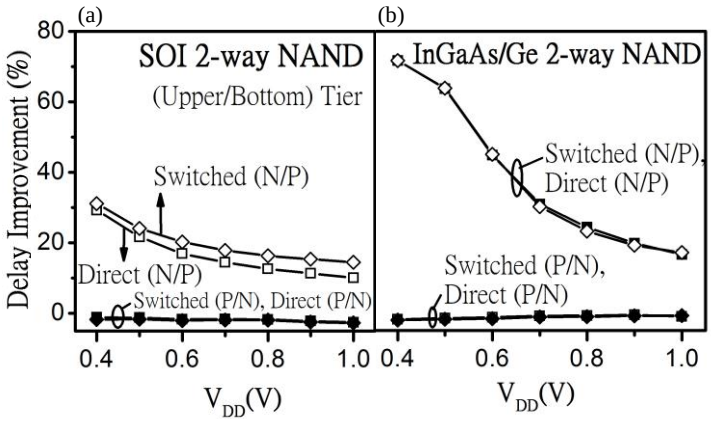

Fig. 9. Performance enhancement of (a) SOI and (b) InGaAs/Ge 3D 2-way NANDs over the 2D counterparts under various tier designs, layouts and V_{DD}.