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# Challenges to the silicon IGBT limit with PNM structure

Masakiyo Sumitomo, Hiroki Sakane, Kazuki Arakawa, Yasushi Higuchi and Masaki Matsui
DENSO CORPORATION Research Laboratories
Nisshin, Aichi, 470-0111, Japan
masakiyo_sumitomo@denso.co.jp

**Abstract**

**A PNM (Partially Narrow Mesa) structure is proposed as a fundamentally new IGBT surface [1]. It is one of the best solutions to approach the silicon IGBT limit performance. It performs the brilliant injection enhancement and can store much carrier in the drift region. So it shows a very low saturation voltage characteristic. By combining the carrier control technology, PNM-IGBT can realize high-speed turn-off. That means it can achieve both very high DC/ AC performance.**

## 1. Introduction

Si-IGBTs are widely used as devices for electric power conversion in consumer electronics, industrial machines, automobiles, bullet trains and so on. Year by year, performance improvements have been achieved through structural improvements. On the other hand, development of power devices using new materials such as GaN and SiC are also going on powerfully. Nowadays they are available in some market. This is why the importance of ascertaining the Si-IGBT practical limit is increasing. To support the expanding electric power demand in the whole world, optimal placement of the power device will be required with high performance and reasonable cost. In this paper, we indicate the Si-IGBT characteristic limitation in the conduction state and switching.

## 2. Conduction State

In conduction state, a lower saturation voltage characteristic is required for lower loss. In 2006, the "Theory of Silicon Limits of IGBTs" was shown by Nakagawa et al [2]. However, the proposed structure was extremely difficult to manufacture. So we propose a fundamentally new structure named PNM-IGBT. Its performance is close to the Silicon Limits (see Fig.1). That does not require any special processes and equipments. Only a few process steps are attached on a conventional trench gate FS IGBT process flow. Fig.2 displays TEM images of the cross-section of the prototypes. The mesa width of samples AC is 0.3, 0.7 and 1.1μm, respectively. Sample D has a conventional trench gate structure (mesa width = 3μm). All samples are composed of a 4μm gate pitch, silicon thickness of 145μm, drift region resistivity of 65Ω·cm and FS backside structure [3]. Fig.3 shows the typical ON state Jc-Vce(sat) characteristics of all prototypes. We confirmed a significant reduction of the saturation voltage in PNM-IGBT. Narrower mesa PNM-IGBT shows lower saturation voltage by its much injection enhancement.

## 3. Turn-off State

In Turn-off state, both of lower energy loss and softer waveform (dI/dt or dV/dt controllability) are required. In fact they are conflicting. So generally we adjust the switching speed by changing the gate input resistance (see Fig.4 black dashed line). Recently, the required switching speed has become higher along with the package technology evolution. However, there is a limit of the loss reduction by this gate resistance control. In this region, the waveform is constrained by the drift region carrier discharge. To cut the loss more, it is necessary to reduce the stored carrier. But it must increase the saturation voltage. They are also conflicting. So we challenged to solve this. Fig.5 shows the illustration of the idea. In the conduction state, it is effective to obtain a modulation effect by using PNM structure. In the turn-off state, we can allow for fast current interruption by reducing the amount of stored carriers. To achieve this, we propose that the positive potential (for continuing the on-state) and the negative potential (for lowering the injection enhancement effect) are respectively applied to the adjacent gate (see Fig.4 blue dashed line). To demonstrate this idea, we have developed a double gate PNM-IGBT. Fig.6 shows the measured waveform. We could reduce the 30% turn-off loss by this technique (also see Fig.4 circle dot).

## 4. Conclusions and Discussions

PNM-IGBT shows a brilliant low saturation voltage. Moreover by controlling the drift region carrier, it performs a very fast current interruption. However, these are not enough for the total system performance. Because paired FWD is also the most important component. SiC-SBD is the best FWD for a loss saving perspective. For a cost reduction, RC-PNM-IGBT must be a powerful solution. PNM-IGBT is very suitable for RC-IGBT (including FWD on one chip) because its good injection enhancement helps to balance IGBT and FWD design.

## Acknowledgements

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## References

[1] M. Sumitomo *et al., "Low loss IGBT with Partially Narrow Mesa Structure", Proceeding of ISPSD2012,* pp17-20

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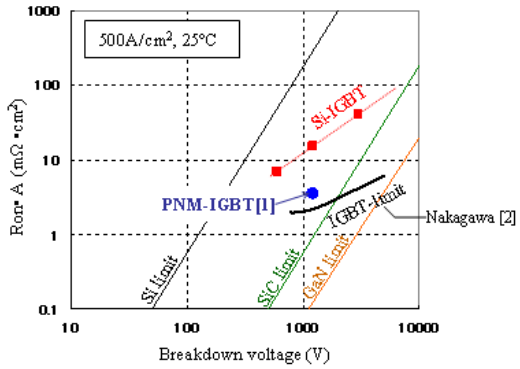


Fig. 1 Relationship between the specific on-resistance and the breakdown voltage

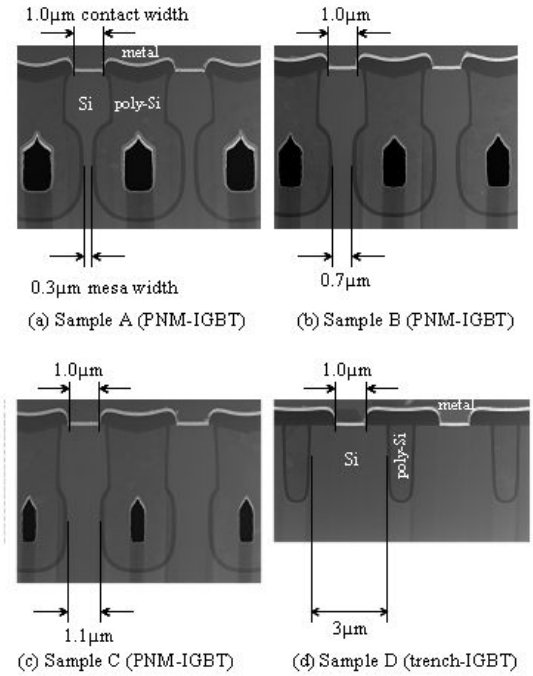


Fig.2 Cross-Sectional TEM images of Sample A-D

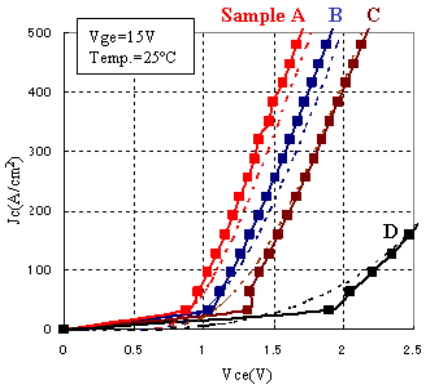


Fig.3 Measured ON state characteristics of Sample A-D
(Dashed lines show simulation results)

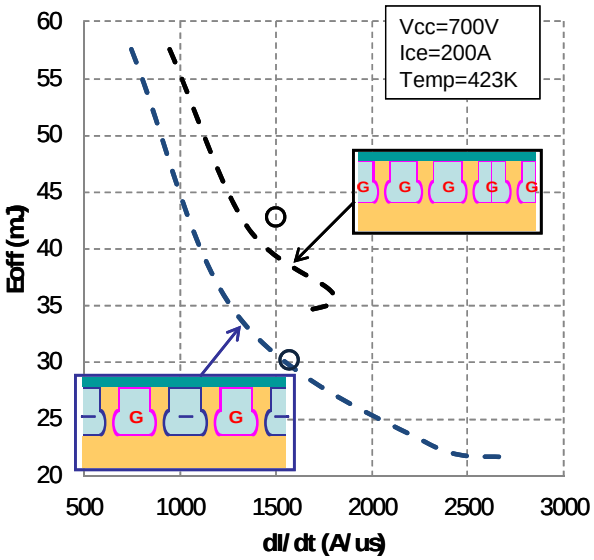


Fig. 4 Relationship between dI/dt and Eoff
(dashed line: simulated with Gate Resistor value
circle dot: measured with Rg=20Ω)

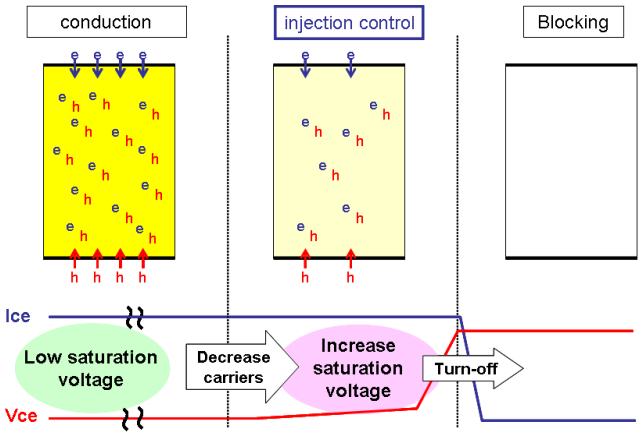


Fig.5 Conceptual diagram of the carrier control technology

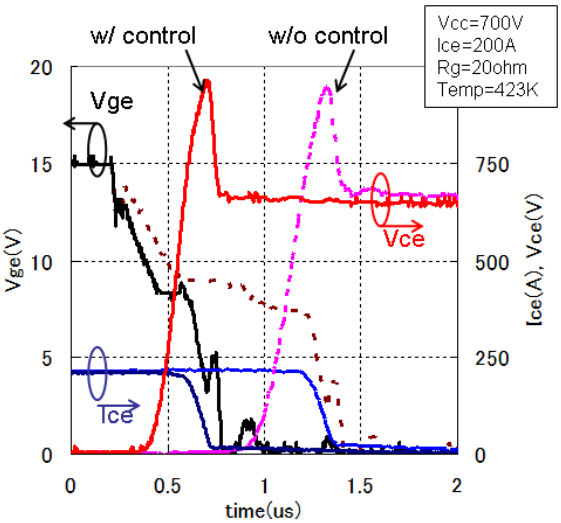


Fig.6 Measured turn-off waveforms
(With-and-Without the carrier control)