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# "Design for EMI suppression" during reverse recovery by 600V lateral SOI PiN diode with traps

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**Abstract**

**PiN diode design for oscillation-induced EMI suppression is proposed with novel structure. The proposed diode is lateral structure with traps using SOI substrate. Conventional PiN diode with vertical structure generates waveform oscillation and the oscillation lower power electronics system reliability. The design of proposed lateral structure with traps will contributes the performance improvement of all of bipolar power devices including IGBT.**

## 1. Suppression of waveform oscillation

The oscillation of proposed lateral diode with traps is successfully suppressed by remained stored carrier throughout the reverse recovery time (see Fig. 1) [1-5]. On the other hand, the strong oscillation is generated by completely swept carrier out of N- layer with the conventional vertical diode regardless of same reverse recovery time and forward voltage drop [6]. The improvement of reverse recovery characteristic is quantitatively indicated by increased Reverse Recovery Softness Factor (RRSF) (see Fig. 2) [7]. The previously-proposed diodes cannot suppress the oscillation because carrier reinjection increases reverse recovery loss or higher doping layer in N- layer acts as N emitter [8, 9].

## 2. Design concept of lateral diode with traps

The conventional vertical diode forms the linearly-sloped electric field distribution corresponding to doping concentration of N- layer at blocking state (see Fig 3). Therefore, the electric field of vertical diode penetrates whole N- layer and sweep stored carrier out of N- layer under the high voltage like surge voltage. The lateral SOI diode with traps has the two electric field peaks at the borders of layers with high electric filed between the peaks. Eventually, the oscillation is suppressed by remained stored carrier in the room for high electric field. The electric field distribution of the proposed diode is formed by positive charge of trapped hole along buried $SiO_2$ side (see Fig. 4).

The traps are designed to make the room with the simple ratio of the trap pitch to the trap height (see Fig. 5). When the ratio is the same, the breakdown voltage is almost equal with similar electric field distribution. The design of proposed lateral SOI structure with traps will widely contributes the performance improvement of bipolar power devices including IGBT.

## References

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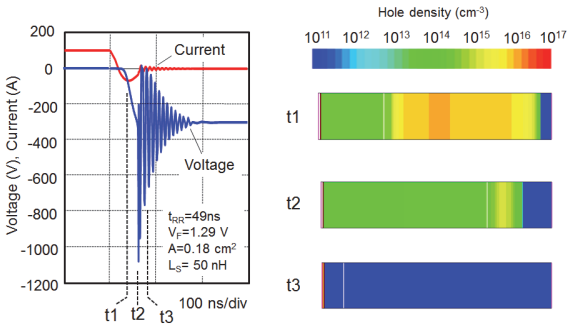
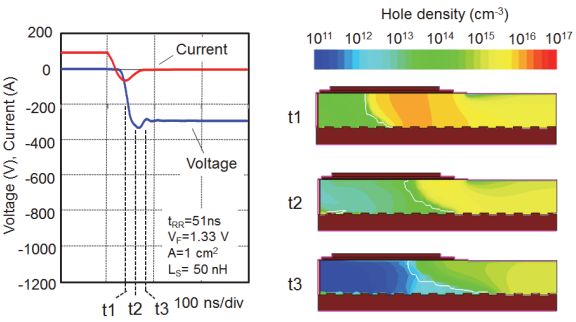



(a) Conventional structure of vertical PiN diode




(b) Proposed lateral SOI PiN diode with traps (Average thickness of silicon and buried $SiO_2$ are 10 μm and 5 μm respectively)

Fig. 1. Waveform during reverse recovery and corresponding hole density by TCAD simulation. Remained hole prevents waveform oscillation.

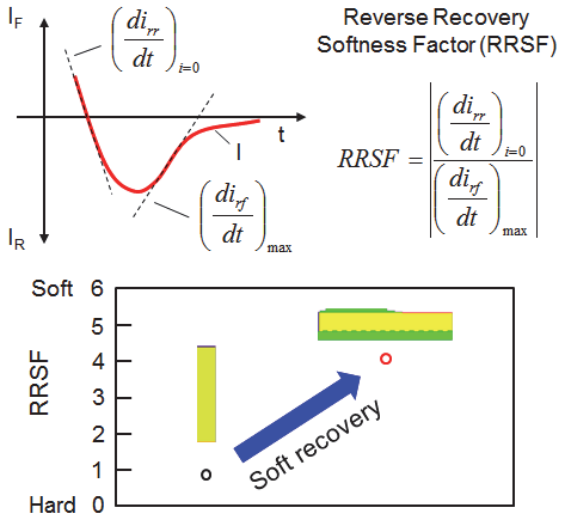
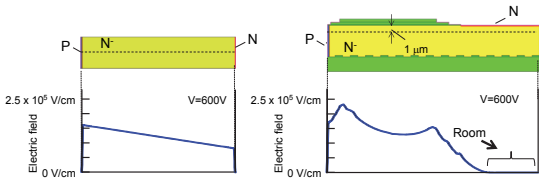



Fig. 2. Reverse Recovery Softness Factor (RRSF) of diodes. RRSF indicates soft recovery of proposed lateral diode compared with conventional vertical diode.




(a) Conventional diode (b) Proposed diode

Fig. 3. Diode structures and corresponding electric field along dotted line by TCAD simulation.

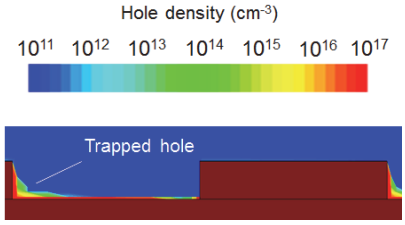
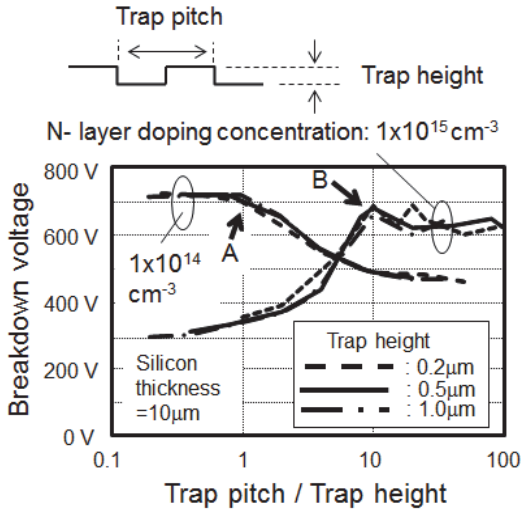
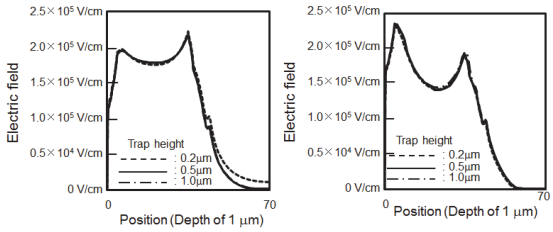



Fig. 4. Trapped hole along buried $SiO_2$ side corresponding with Fig. 3. (b).




(a) Breakdown voltage change with trap design




(b) Electric field at "A" (c) Electric field at "B"

Fig. 5. Breakdown voltage change by trap design.