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An 800V-Class Lateral NMOS Structure with a Reduced Parasitic Capacitance for a Level-Shift Circuit Integrated in a High Voltage Gate Driver IC

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Abstract

A new 800V-class lateral NMOS structure with a drastically reduced parasitic capacitance (C_{oss}) has been developed for integration in a high voltage gate driver IC. In our new device a 40% reduction of the C_{oss} from the conventional one can be achieved by using two n-type drift regions divided by a p-type diffusion layer.

1. Introduction

High voltage ICs (HVICs) [1] for driving the gates of power devices arranged in a bridge circuit configuration are intended to develop power supply systems [2, 3]. This is because the energy savings in power supply systems can be achieved by using the HVIC. One of the most important parameters of the HVIC to achieve the energy saving is the I/O propagation delay time, which dominates driving performances of low-side and high-side power devices in a bridge circuit. The shorter I/O propagation delay time is required.

For the shorter I/O propagation delay time of the HVIC, a parasitic capacitance (Coss) of a high voltage NMOS (HVNMOS), which is used for a level-shift circuit (lever shifter) integrated in the HVIC, must be suppressed. However, it is very difficult to decrease the Coss of the HVNMOS because the HVNMOS has the large pn junction area to maintain the high blocking capability.

In order to decrease the I/O propagation delay time, we have proposed a new lateral 800V-class HVNMOS with a reduced parasitic capacitance, which is called as a RPC_HVNMOS in this paper, for a level shifter integrated in an 800V-class HVIC. The unique point of this device is including the floating potential region in the n-drift region to reduce the Cdsub, which is a component of the Coss. A 40% reduction of the Coss can be accomplished experimentally compared from the conventional HVNMOS. And by using the RPC_HVNMOS we have confirmed that the I/O propagation delay time of the fabricated HVIC is about 12% shorter than that of the HVIC integrating the conventional device. This paper describes the concept of our proposed RPC_HVNMOS structure and shows numerical and experimental results.

2. I/O propagation delay time of the HVIC

Figure 1 shows a block diagram of the HVIC circuit [3]. High-side and low-side driver circuits, level shifter, an input control circuit and so on are integrated in the HVIC. The total delay time occurred in all component circuits becomes the I/O propagation delay time of the IC.

From our analysis it is found that the delay time occurred in the level shifter accounts for about 30% of the I/O propagation delay time of the 800V-class HVIC. This is because the 800V-class HVNMOS, has the large Coss induced by the large pn junction area in the device. Therefore, the Coss of the HVNMOS must be suppressed sufficiently low to shorten the I/O propagation delay time of the IC.

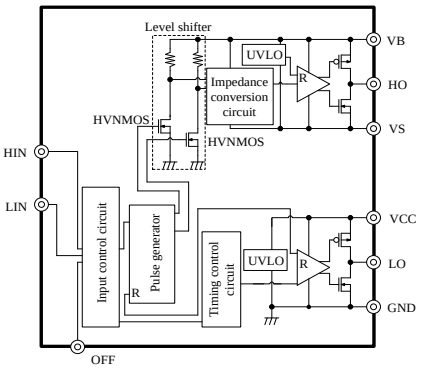

Fig. 1 Block diagram of the HVIC circuit.

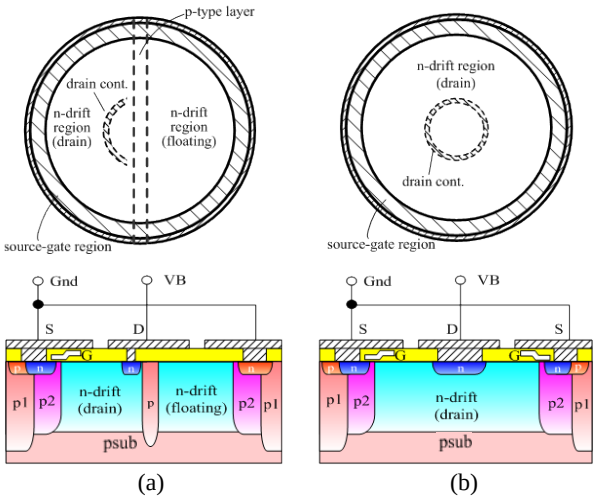

Fig. 2 P1ane views and cross sections of (a) RPC_HVNMOS and (b) conventional HVNMOS structures.

3. Device Concept and Results

Figures 2 (a) and (b) show RPC_HVNMOS and conventional HVNMOS structures, respectively. Both devices are formed on a p-type substrate and have the cell pattern with the drain region surrounded by the source-gate region. Figure 3 shows the C-V simulation results of the conventional device. From these results it is found that the Cdsub, which consists of the junction between a p-type substrate and the n-type drift region, is the largest in the Coss of the device.

The original point of our proposed RPC_HVNMOS structure to reduce the Cdsub is to divide the n-drift region into the drain voltage applied region and the floating potential region by the p-type diffusion layer reaching the p-type substrate, as shown in Fig. 2 (a).

The p-type diffusion layer for the separation of the n-drift region is depleted with increasing the drain voltage, so that the blocking capability of the device can be maintained. Figures 4 (a) and (b) show simulation results regarding an off-state characteristic and the potential distribution when the avalanche breakdown occurs in the device, respectively. The breakdown voltage of 830V can be obtained from the RPC_HVNMOS.

We have fabricated the RPC_HVNMOS using a p-type substrate. Figure 5 shows I-V characteristics of a fabricated device. As shown in Fig.5, the blocking capability under the Vg of 5V is over 800V. Figure 6 shows the C-V curves of the fabricated device. In this figure the result of the conventional HVNMOS device fabricated together with the RPC_HVNMOS is plotted. The Coss of the RPC_HVNMOS under the Vd of 0V is 40% lower than that of the conventional device. The I/O propagation delay time (Tdon, Tdoff<60ns) of the fabricated HVIC with the RPC_HVNMOS is 12% shorter than that of the HVIC with the conventional device. We have succeeded in shortening the I/O propagation delay time of the HVIC by using our proposed RPC_HVNMOS.

4. Conclusions

This paper presents new lateral 800V-class HVNMOS with the reduced parasitic capacitance for the level shifter in the HVIC. The new device has two n-type drift regions divided by the p-type diffusion layer reaching the p-type substrate, in order to reduce the Cdsub. One n-drift region is set as floating potential.

We have succeeded in a 40% reduction of the Coss compared with that of the conventional device. This can be done without sacrificing the blocking capability of the device. By applying our proposed HVNMOS to the HVIC we have realized 12% shorter I/O propagation delay time of the HVIC.

References

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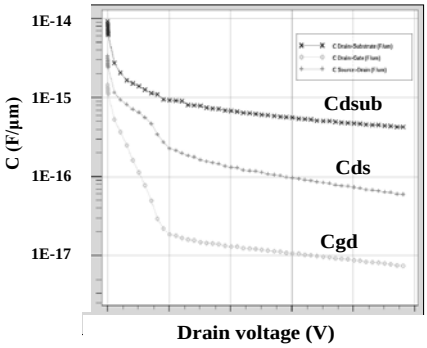


Fig. 3 C-V simulation results of the conventional HVNMOS.

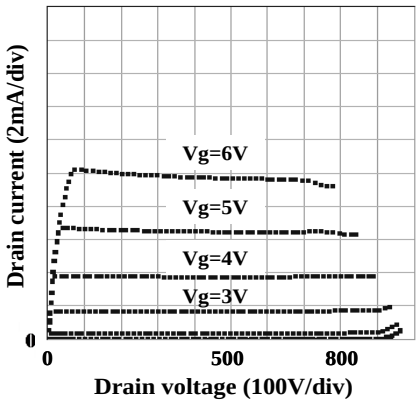
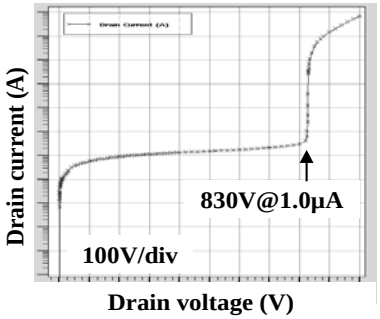
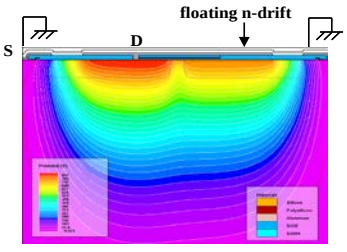


Fig. 5 I-V characteristics of a fabricated RPC_HVNMOS.



(a)



(b)

Fig. 4 Simulation results regarding (a) an off-state characteristic and (b) the potential distribution of the RPC_HVNMOS.

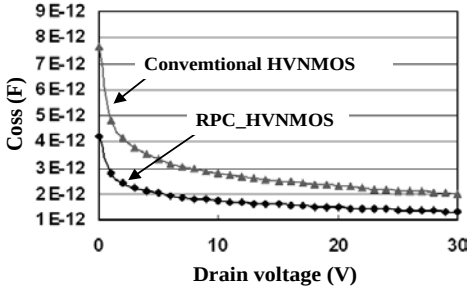


Fig. 6 C-V curves of the fabricated devices.