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250°C Switching Behavior of All SiC Power Module with Sandwich Structure

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Abstract

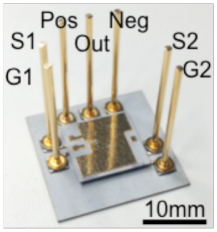
A wire-bond-less all SiC power module with sandwich structure is demonstrated. The circuit configuration of the module is 2-in-1, consisting of two SiC-junction field effect transistors (JFETs) and two SiC-Schottky barrier diodes (SBDs) which are arranged between two ceramic circuit boards. The double pulse switching test at 250°C is successfully carried out with 600 V, 15 A, and over 10 V/ns switching speed is realized.

1. Introduction

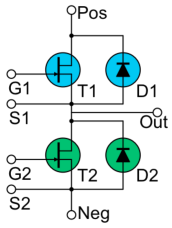
Silicon carbide (SiC) power devices are expected to operate under high temperature and speed compared to conventional Si power devices [1]. The SiC power modules can reduce the size of cooling devices and filter components [2]. The sandwich structure module can reduce the parasitic inductance and can improve cooling capability [3]. In our previous research, the all SiC power module with sandwich structure was designed and manufactured. By introducing symmetrical pattern circuit boards, the thermal cycle of 500 cycles was achieved in the temperature range between -40°C and 250°C [4]. The module switching characteristics were confirmed at room temperature [5]. In this paper, the results of double pulse test at 250°C are shown.

2. Sandwich structure power module

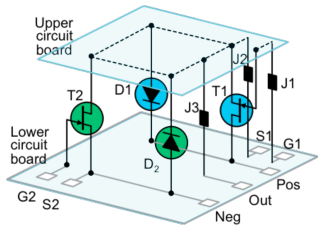
The manufactured SiC power module with sandwich structure is shown in Fig. 1(a). Two silicon nitride-active metal brazed copper (SiN-AMC) ceramic circuit boards are used. Between these circuit boards, two JFETs (T1, T2: SemiSouth, SJEC120R050, rating 1200 V, 30 A at 25°C) and two SBDs (D1, D2: SemiSouth, SDC30S120, rating 1200 V, 30 A at 25°C) are integrated as shown in Fig. 1(b). The module size is 2 × 2 × 0.2 cm (0.8 cm^3) except terminal pins. To minimize the inductance between Pos pin and Neg pin, the length of the main current path is reduced by introducing the three-dimensional (3D) layout as shown in Fig. 1(c). The source pad of T1 is connected to the drain pad of T2 on the upper circuit board. As the gate and source pads of the T1 and T2 are bonded precisely to the circuit board, the flip-chip technique is used [4]. Fig. 1(d) shows the upper and lower circuit boards with the devices. These circuit boards are combined by reflow bonding technique.



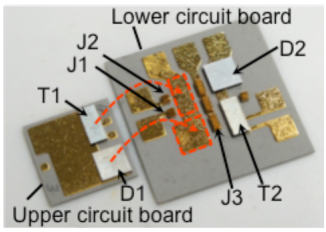
(a) Manufactured module.



(b) Circuit diagram.



(c) 3D device configuration.



(d) Lower and upper circuit boards with devices.

Fig. 1 Sandwich structure of all SiC power module.

3. Double pulse test setup

The circuit diagram for the double pulse test is shown in Fig. 2(a). The terminal pins of the module are mounted to the test fixture board as shown in Fig. 2(b). Two micro ceramic heaters are attached to both sides of the module as shown in Fig. 2(c). Both upper and lower circuit boards temperature are measured by using thermocouples in order to control the device temperature. T2 is drove by the commercial gate driver (SemiSouth, SGDR600P1) is used. The external inductance L of 1 mH is used for load. To maintain the T1 in the off state, G1-S1 is continuously biased to -15 V. The parasitic inductance in the module L_{P1} + L_{P2} is measured to be 4.7 nH using impedance analyzer (Agilent 4294A). It is significantly smaller than the conventional module, whose parasitic inductance is several tens of nH, due to the wire-bonds (e.g., over 10 nH for TO-247). The parasitic inductance L_S of the Pos-C-Neg path is also measured to be 8.8 nH. Thus the total inductance of the loop between the module and C is 13.5 nH.

4. Switching behavior at 250°C

To investigate the switching behavior, the double pulse test is carried out. The sequence is shown in Fig. 3; (a) the 1st pulse charges up the inductor current to the desired value,

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(b) the inductor current circulates through the freewheel diode D1 immediately after T2 turns off, (c) the 2nd pulse is generated by T2 turn-on (turn-on behavior is measured), (d) the current of T2 is commutated to the freewheel diode D1 (turn-off behavior is measured).

The module temperature is controlled to 250°C. V_{DC} is set-up by 600 V. The 1st pulse width is 20 μs and the 2nd pulse width is 5 μs, the delay time between the pulses is 30 μs. Under this condition, the turn-on behavior of T2 at the load current I_L of 12 A, and turn-off behavior at 15A are measured. The drain-source voltage V_{DS2} of T2 is measured between the Neg pin and the Out pin. The drain-source voltage V_{DS1} of T1 is obtained between the Out pin and the Pos pin. The gate voltage V_{GS} of the T2 is measured between the S2 pin and the G2 pin. The measurement results are shown in Fig. 4. The module at 250°C successfully switches under conditions of the 600 V, 15 A. The details of the turn-on and turn-off switching waveform is shown in Fig. 4(b) and Fig. 4(c). The maximum transient speed (dV/dt) of the turn-on and turn-off are 10.7 V/ns and 12.1 V/ns, at the current of 12 A and 15 A. Almost no surge voltage is observed even if the turn-off speed is 12.1 V/ns, due to the low parasitic inductance of the module.

4. Conclusions

The proposed all SiC power module with sandwich structure has the characteristics of low inductance of 4.7 nH due to the short circuit path configuration and wire-bond-less interconnection. The module is successfully operated at 250°C with almost no surge voltage even if the turn-off speed is high (12.1 V/ns at the current of 15 A).

The 250°C switching operation of the power module presented in this paper indicates the significant reduction of the size of cooling devices. Furthermore, the sandwich structure all SiC power module introducing the three-dimensional (3D) layout has low parasitic inductance, resulting in the high speed switching behavior. This means the size reduction of the filter components can be achieved. Thus, the drastic miniaturization of the power converter can be expected.

Acknowledgements

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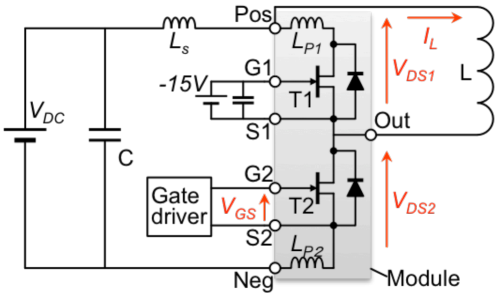
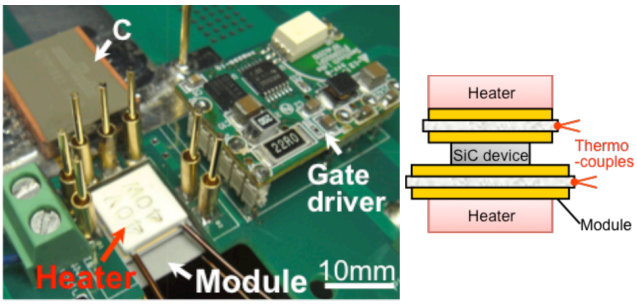
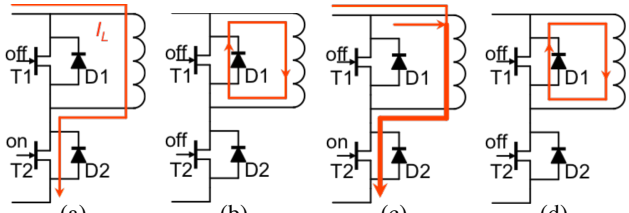


(a) Circuit diagram of double pulse test.



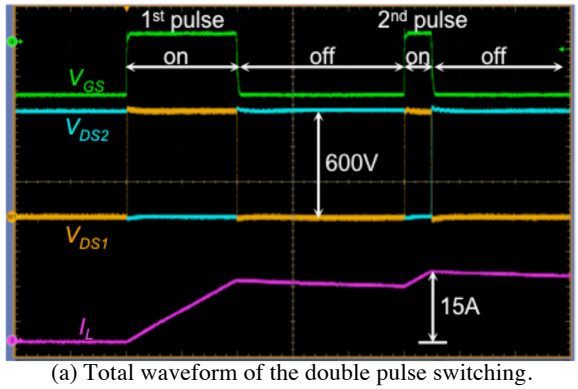
(b) Test fixture with double side heating. (c) Heaters setup.

Fig. 2 High temperature switching test setup.

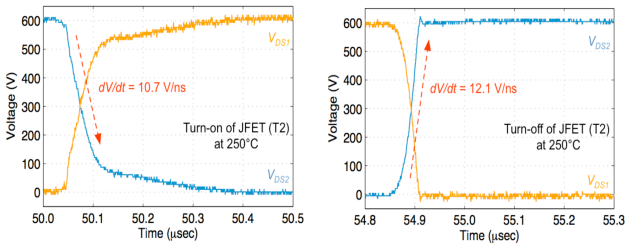


(a) 1st on state (b) 1st off state (c) 2nd on state (d) 2nd off state

Fig. 3 Double pulse test sequence.



(a) Total waveform of the double pulse switching.



(b) 2nd turn-on waveform (c) 2nd turn-off waveform

Fig. 4 Measurement waveforms of 250°C double pulse test.