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Accurate Physical Compact Models of High-Voltage/Power Semiconductor Devices for Efficient Design of Performance-Optimized Circuits and Systems

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Abstract

The compact high-voltage/power device models of the HiSIM family are reviewed. Special focus is given on the HiSIM_HV model for integrated lateral high-voltage MOSFETs as e. g. the lateral double-diffused MOS (LDMOS) and its extension to vertical power-device structures like UMOS or SJ-MOS. Further extension to advanced materials like SiC and reverse/forward recovery effects are also discussed.

1. Introduction

Accurate compact models of power semiconductor devices are an indispensable asset throughout the electronics industry enabling accurate and reliable simulation/design of electronic circuits [1]. The dynamic device and circuit behavior, in particular during device switching, requires accurate capturing of intrinsic device capacitances, which can only be achieved by a device-physics-based modeling with as few approximations as possible. The surface-potential modeling concept has emerged during the last 10 years as the most successful approach for this purpose. It is applied in nearly all recent industry-standard models of MOS-based devices. The HiSIM compact-model family is a prominent representative of this approach and extends it to a more general potential-based modeling concept, which can cover in particular also high-voltage/power devices as e.g. high-voltage MOSFETs or IGBTs [2].

Until recently, accurate compact models were in low demand for the design of power-electronic circuits because dynamic behavior was mainly determined by external capacitances/inductances, exact switching waveforms were unimportant due to low switching frequencies and power losses were mainly determined by the static on-resistance of the power devices. Now these traditional boundary conditions change as higher switching frequencies are essential for modern low-loss power circuits, needed in many applications like automotive electronics, mobile communication or power conversion/conditioning in smart grids with renewable energy sources. In addition to the standardization of other HiSIM models, such trends resulted in the selection of HiSIM_HV as international industry-standard model for high-voltage MOSFETs [1]. The development of HiSIM family models for many other power-device types is carried out in cooperation with the Japanese power-electronics industry. Here we review the status of HiSIM compact models for power-semiconductor devices.

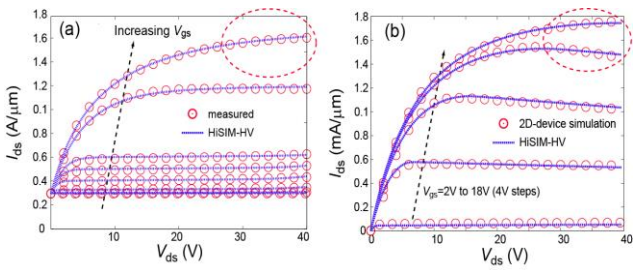

Fig. 1. Fitting results of quasi-saturation and self-heating with HiSIM_HV2, including spatial variation of power dissipation, for the *I-V* characteristics of long L_{drift} devices (measured and TCAD data) verifying accurate reproduction, also for large V_{gs}.

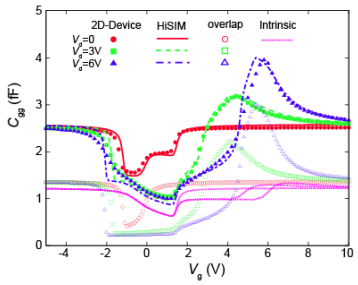

Fig. 2. Bias-dependent gate capacitance C_{gg} as calculated with HiSIM_HV and 2D device simulation. Decomposition into overlap and intrinsic contributions verifies the overlap-capacitance responsibility for anomalous peaks with much higher values than the oxide capacitance.

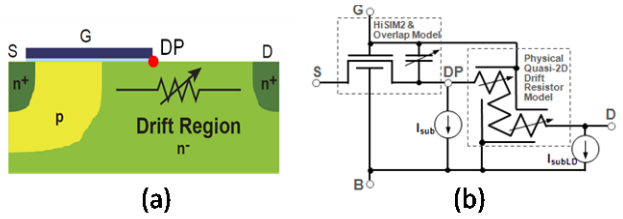

Fig. 3. Simplified LDMOS structure (a) and simplified HiSIM_HV2 equivalent circuit diagram (b).

2. HiSIM_HV and its Derivative Models

The important distinctive properties of the lateral high-voltage MOSFET (LDMOS) are (*i*) a quasi-saturation effect in the current-voltage characteristics I_{ds}-V_{ds} for higher gate voltages V_{gs}, (*ii*) a strong self-heating effect complicated by spatial variation of the power dissipation (Fig. 1), and (*iii*) anomalous peaks in the gate capacitance C_{gg} (Fig. 2). These features originate from bias-dependent resistance properties of the drift region (see simplified LDMOS structure in Fig. 3a), which are modeled in HiSIM_HV by introduction of an internal node DP at the end of the overlap capacitance between gate and drift region. The potential at DP is obtained by a consistent solution for the potential distribution from source to drain contact (Fig. 4). Fig. 3b depicts the obtained equivalent circuit of the HiSIM_HV

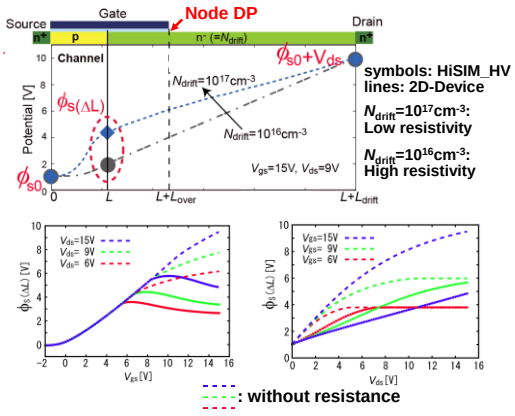

Fig. 4. Comparison of potential distribution from source to drain, as determined with HiSIM_HV and 2D-device simulation for low and high drift-region doping (upper part). The effect of drift-region-resistance consideration on internal potentials at the channel end as a function of V_{gs} and V_{ds} is shown in the lower graphs.

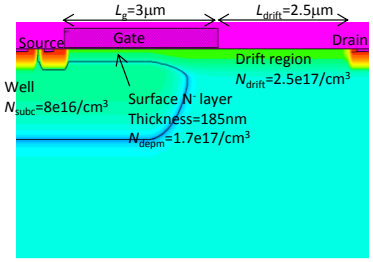

Fig. 5. Typical depletion-mode n-channel LDMOS transistor structure.

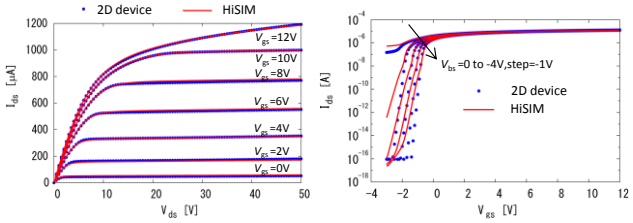

Fig. 6. I_{ds}-V_{ds} characteristics at V_{bs}=0V (left) and I_{ds}-V_{gs} characteristics at V_{ds}=0.1V (right). Depletion-mode transistor width and length are W=1µm and L=3µm, respectively.

model framework, which additionally includes quasi-2D drift-region modeling [3]. Figs. 1 verifies that the outlined modeling approach enables accurate reproduction of (*i*) and (*ii*). Fig. 2 shows the verification for (*iii*). Furthermore, HiSIM_HV provides model scalability with internal MOSFET length and width as well as drift-region length and doping level. Continuous derivatives of *I-V* and capacitance characteristics up to several orders are also provided.

Normally-on or depletion mode devices (see Fig. 5), for which no accurate compact models exist, are used in many practical high-voltage circuits. For relieving this problem, a high-quality depletion-mode model option is included in the latest version (2.2.0) of HiSIM_HV, enabling accurate reproduction of I-V and capacitance characteristics, as verified in Figs 6 and 7, respectively.

The trench high-voltage MOSFET or UMOS is a main-stream structure for discrete devices with vertical MOSFET-orientation and current flow. Many identical cells are connect in parallel on the whole chip to achieve very low on resistances. Fig. 8 shows a typical UMOS half-cell. In comparison to the lateral LDMOS, important additional properties to be captured are trench-width dependent modifications of the 2D current flow as well as modifications in the temperature dependence of *I-V* and capacitance characteristics. As examples, 2D-device simulation and compact model results for I_{ds} and output conductance g_{ds} are compared at elevated temperature of 400° K in Fig. 9.

A favored high-voltage MOSFET structure for the application range up to 500V is the super-junction (SJ)

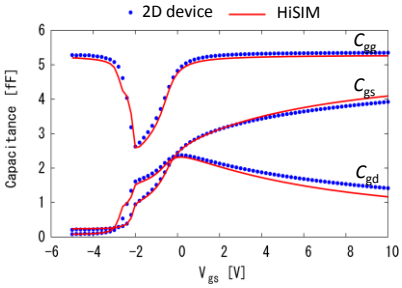

Fig. 7. C_{gg}, C_{gs}, and C_{gd}, characteristics (W=1µm, L=3µm) as a function of V_{gs} at V_{ds}=0V and V_{bs}=0V for the depletion mode LDMOS transistor. HiSIM_HV results are compared to 2D device simulation.

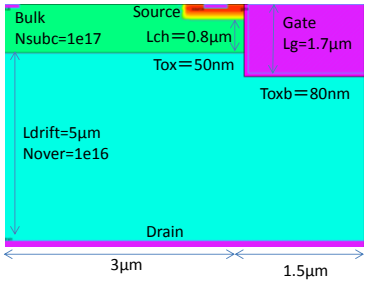

Fig. 8. Typical UMOS cell structure for vertical high-voltage MOSFETs.

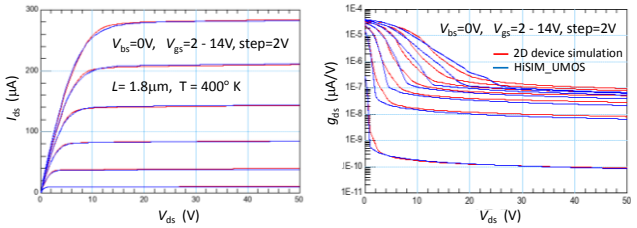

Fig. 9. I_{ds}-V_{ds} characteristics at V_{bs}=0V (left) and corresponding output conductance g_{ds}-V_{ds} characteristics (right) at 400°K temperature. UMOS transistor width and length are W=10µm and L=1.8µm, respectively.

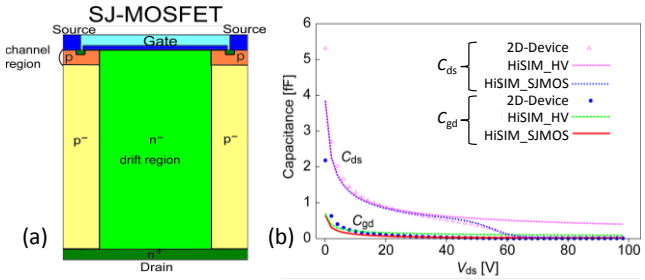

Fig. 10. SJ-MOSFET structure (a) and capacitance reproduction of the SJ-MOSFET with HiSIM_SJMOS in comparison to 2D-device simulation and HiSIM_HV results (b).

MOSFET, which features high switching speed and low switching energy due to its reduced capacitances at high V_{ds}. Fig. 10a depicts the SJ-MOSFET structure with its pillar p⁻-regions, extending vertically from source to drain. The typical abrupt capacitance reduction of the SJ-MOSFET can be well reproduced with the developed potential-based model extension of HiSIM_SJMOS as demonstrated in Fig. 10b [4].

Further applications of the HiSIM compact model concept for high-voltage/power devices, including the IGBT structure, utilization of advanced semiconductor materials like SiC and compact modeling of reverse/forward recovery, will be described in the presentation.

3. Conclusions

Potential based compact models of the HiSIM family for high-voltage/power semiconductor devices have been reviewed. Due to their optimized trade-off between accuracy and calculation time, these models have evolved into the industry standard models in recent years.

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