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Two-Component Model for Threshold Voltage Shifts of SiC MOSFETs under Negative Bias Stress

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Abstract

Negative bias temperature instability in SiC MOS FETs was investigated. Threshold-voltage shift was explained using the sum of two components. One component has reverse-temperature dependence possibly due to existing traps and causes short term instability. The other component has forward- temperature dependence and time dependence in power law with a power index similar to that of Si devices. We show that control of the latter component is important for long-term stability.

1. Introduction

To realize highly reliable SiC MOS power devices, the instability of the threshold voltage, V_{th}, under negative gate bias stress is a critical issue. This is because negative bias causes negative shift of V_{th}, and the negative shift results in an increase in off-current, which degrades the breakdown voltage [1]. In this paper, we discuss the time dependence of ΔV_{th} under stress. We consider the transient response of existing traps and activation of additional traps to explain the kinetics of ΔV_{th}. Based on this consideration, we propose a two-component model. We also discuss the origin of the additional trap with respect to the time dependence. N- or H-related sites are suggested as possible origins.

2. Experimental

We used conventional SiC DMOSFETs. The FETs were fabricated on Si-face 4H-SiC substrates with n-type epi-layers. After the ion implantation processes, activation annealing was performed. Then, gate oxides, poly-Si-gate electrodes, and inter-layer dielectric films were formed. Finally, metallization processes were performed.

In the stress tests, a V_g-I_d sweep and bias stress were alternately performed. The width of the sweep was limited to 3 V around the V_{th} to suppress additional shifts during the sweep. V_{th} was defined as the gate voltage at which the I_d reaches 2 pA/μm with a drain-source bias of 50 mV. Drain and source were grounded during the stress period.

3. Results

Figure 1 shows typical ΔV_{th} under a negative bias with a linear scale. The shift was negative, indicating an increase in positive charge due to trapping of holes. With a log time scale (Fig. 2), the absolute shift appears to have two phases. In the short term, the increase of the shift is small. In the long term, the increase of the shift is larger. The temperature dependence of the ΔV_{th} kinetics is shown in Fig. 3. In the short term, the shift shows reverse-temperature dependence. Additional increase in the long term shows forward temperature dependence. Figure 4 shows the stress-bias dependence of the ΔV_{th} kinetics. Additional increase in the long term shows clearer bias dependence.

4. Discussion

Considering the slow-oxide trap of SiC-MOSFET that was reported for a transient current response to step-gate bias operation [2], we think that ΔV_{th} kinetics has two components that are caused by the different types of trap. The first component that mainly governs the characteristics in the short-term corresponds to the existing trap (i.e. slow-oxide trap). The second component that mainly governs the characteristics in the long-term was considered to be caused by additional activation of traps at SiC-SiO_2 interface. Because the first component has small stress-time dependence, which is well consistent with the physical image of the transient response, we modeled ΔV_{th} as follows.

$$|\Delta V_{th}| = A + B \cdot t^n \qquad (1)$$

Using this model, we fitted the data of Fig. 3 and 4 as shown in Fig. 5 and 6. The model well expressed the ΔV_{th} behavior at the various temperatures and biases. Parameter A showed reverse-temperature dependence while parameter B showed forward-temperature dependence (Fig. 7(a)). This is because the time constant of the transient response of the existing traps was not so large at high temperature that trapped charges were emitted or recombined during the interval between the stress and the sweep. Also, the forward-temperature dependence of B suggests that additional traps were thermally activated. Parameter B depends on the stress bias while dependence of parameter A is small (Fig. 7(b)). This suggests that the activation mechanism of the additional traps was strongly enhanced by the bias.

According to our model, the power index, n, can provide the suggestion for the origin of the additional traps. As shown in Fig. 5 and 6, we obtained the power index n = 0.19 for all data. This power index is in the range of power indices of Si device, n = 1/4-1/6 [3-5]. Therefore, we consider that the origin of additional traps might be similar to that of Si device, namely, H-, or N-related sites [3-5]. This implies that the excess nitridation of the SiC-SiO_2 interface degrades the BTI of SiC MOSFETs.

Finally, Fig. 8 shows long-term prediction using our model and simple power law. Because the charge emission from the existing traps is not considered, the simple power law underestimates the shift. For long-term estimation of ΔV_{th} of SiC MOSFETs, both components should be taken into account.

5. Conclusion

ΔV_{th} of SiC MOSFETs under negative bias stress was investigated. The model considering existing and additional traps fitted the data well. The additional component showed time dependence in power law. The obtained power index is in the range of power indices of Si devices, suggesting that possible origins are N- or H-related sites. Controlling such trap sites is important for long term stability.

References

[1] A. J. Lelis et al., Mater. Sci. Forum, **599** (2011) 679.

[2] S. Potbhare et al., IEEE Trans. Electr. Dev. **55** (2008) 2061.

[3] S. Bhardwaj et al., IEEE CICC (2006) 189.

[4] Y. Mitani et al., IEEE Trans. Dev. Mat. Rel., **8** (2008) 6.

[5] P. Lenahan et al., IEEE Trans. Dev. Mat. Rel., **11** (2011) 219.

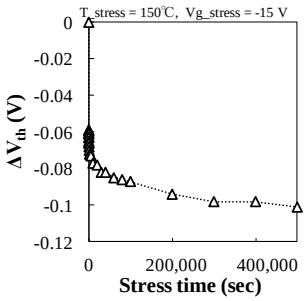

Fig. 1 Time dependence of typical ΔV_{th} of a SiC MOSFET under a negative bias.

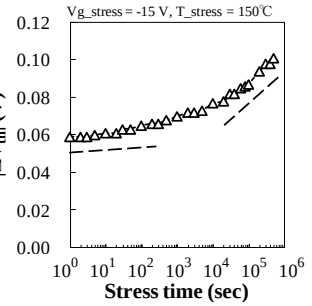

Fig.2 ΔV_{th} of a SiC MOS FET under a negative bias with a log time scale.

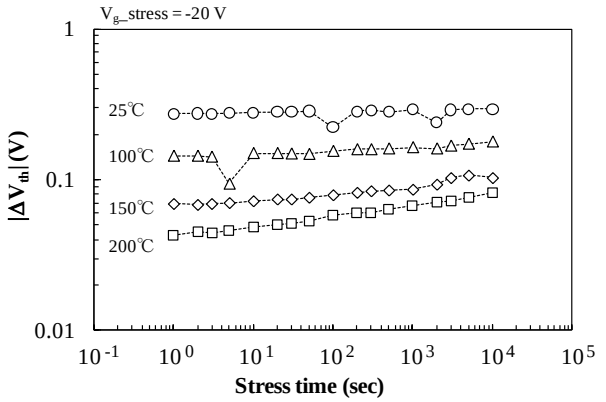

Fig. 3 Time dependences of ΔV_{th} of SiC MOSFETs at varied temperatures.

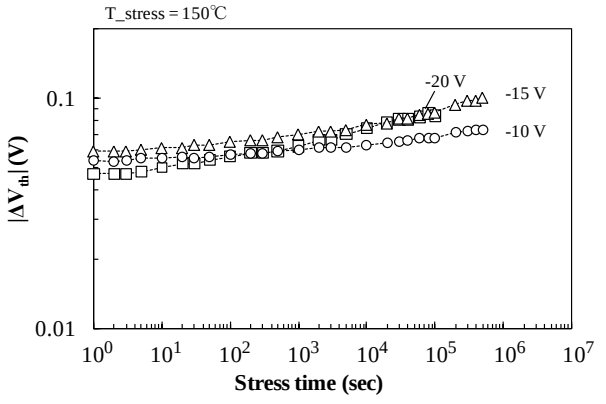

Fig. 4 Time dependence of ΔV_{th} of SiC MOSFETs under various negative stress biases at stress temperature of 150℃.

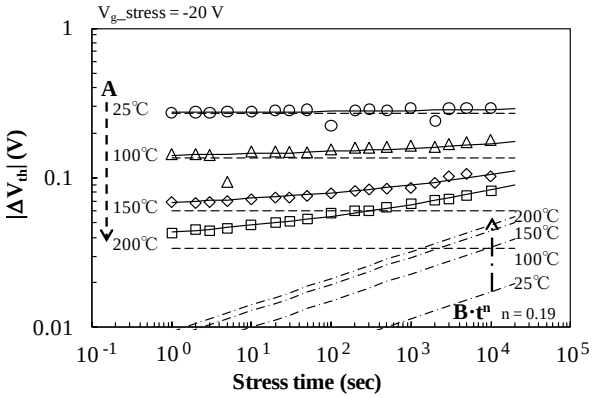

Fig. 5 Time dependences of ΔV_{th} of SiC MOSFETs at varied temperatures.

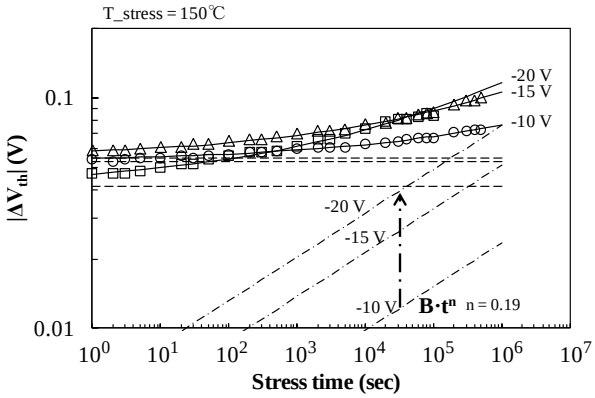

Fig. 6 Time dependence of ΔV_{th} of SiC MOSFETs under various negative stress biases at stress temperature of 150℃.

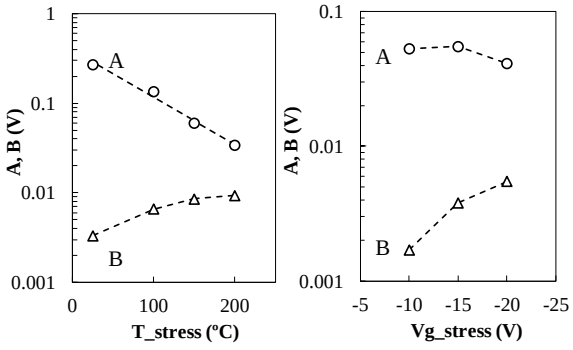

Fig. 7 (a) Temperature and (b) bias dependence of parameters A and B.

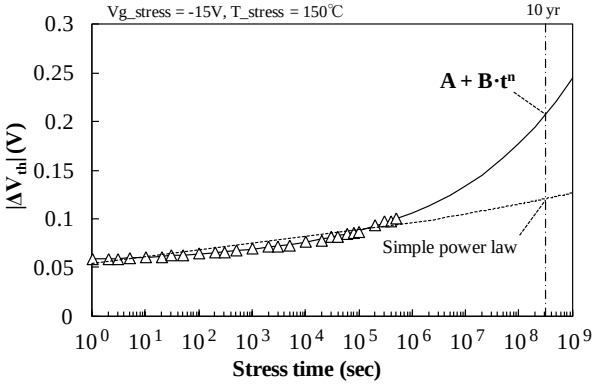

Fig. 8 Long term estimation of ΔV_{th} of SiC MOSFET under negative bias using two-component model.