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Encapsulated Gate-All-Around InAs/InP Core-Shell Nanowire FETs

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Abstract

Field-effect transistors are fabricated using an optimized gate-all-around gate-overlap structure and an InAs/InP core-shell nanowire channel. Superior subthreshold properties are observed, compared to similar homogeneous InAs NW-FETs. Post-annealing is found to improve the subthreshold properties of the FET, which is ascribed to the formation of InAlAs alloy at the interface between the InAs core and Al source/drain electrodes.

1. Introduction

Semiconductor nanowires (NWs) grown by the vapor-liquid-solid (VLS) method are the subject of intense study due to their potential application to the next generation of nanoelectronic devices. InAs NWs are of particular importance in view of application to high-speed, low-power-consumption field-effect transistors (FETs) due to their high intrinsic electron mobility. Moreover, the cylindrical shape of self-assembled NWs is suitable for implementing gate-all-around (GAA) geometry, where the channel is completely surrounded by the gate, thereby offering improved electrostatic control and reduced short-channel effects [1].

In this work, we report the DC electrical characteristics of InAs/InP core-shell NW-FETs with an optimized GAA gate-overlap geometry, measured before and after annealing. We have previously reported the fabrication of encapsulated GAA InAs NW-FETs using a two-step gate electrode formation method, which led to a dramatic improvement in on-state properties due to reduced parasitic resistance [2]. The use of an InAs/InP core-shell NW as a channel material is known to reduce ionized impurity and surface roughness scattering, improving the field-effect mobility by a factor of 2-5 over homogeneous channel InAs NW-FETs [3, 4]. Here, we fabricate a GAA FET using an InAs/InP core-shell NW channel whose source/drain electrodes consist of self-aligned stacks of SiO_x/Al/SiO_2, which enables further down-scaling of the gate length.

2. Experimental method and results

InAs NWs are grown via the Au-catalyzed VLS mode, with an InP shell grown by vapor phase epitaxy in a MOVPE system. The as-grown NWs are wet-etched in diluted HCl inside a glove box with an oxygen concentration of less than 0.1 ppm. The NWs are then conformally coated with 5 nm of Al_2O_3 via atomic layer deposition (ALD). Pre-ALD wet-etching removes part of the InP shell along with natural oxides on the NW surface, resulting in a ~ 5 nm shell thickness, which is confirmed by transmission electron microscopy.

The NWs are then transferred onto a Si/SiO_2 device substrate that is prepatterned with the Ti/Au lower gate electrode and source/drain leads. Figure 1(a) and 1(b) schematically show the device structure and its cross-section along the NW axis, respectively. The source/drain regions are defined by simultaneous electron beam lithography of hydrogen silsesquioxane (HSQ) and polymethyl methacrylate (PMMA) on top of it. HSQ turns into SiO_x by this electron beam irradiation. After removing the surface oxides and the InP shell by Ar plasma-etching using the developed PMMA as a mask, Al and SiO_2 are deposited in sequence. After the lift-off of the Al and SiO_2 layers, unexposed HSQ is removed in Tetramethylammonium hydroxide (TMAH), leaving SiO_x only below the Al/SiO_2 layers. This self-aligned SiO_x serves to electrically isolate the Al source/drain layer from the lower gate metal, while maintaining an Ohmic contact between the Al and the NW channel. As the final step, the upper gate metal is deposited, overlapping the source/drain electrodes and realizing the GAA structure. Figure 1(c) shows a scanning electron microscope (SEM) image of the fabricated NW-FET device with the gate length (equal to source-drain separation) L_g = 1.75 μm and the NW diameter d = 120 nm.

DC electrical characterization of the NW-FETs was performed at room temperature. The dashed lines in Fig. 2 show transfer characteristics of the as-fabricated device at drain voltage V_d = 100 mV, in both linear and logarithmic scale. From the observed maximum transconductance of g_m = 7.5 μS, field-effect mobility is calculated to be μ_{FE} ~ 300 cm^2/Vs by the routinely used expression, $\mu_{FE} = L_g^2 g_m / C_g V_d$, where C_g is the gate capacitance. A two-layer dielectric coaxial capacitor model is used to evaluate the gate capacitance, neglecting other contributions such as quantum capacitance and interface state capacitance. This simplification implies that the deduced gate capacitance is overestimated [5], and the above value should be regarded as a lower bound for the actual mobility.

A subthreshold swing (SS) of 180 mV/decade is observed, which is three-times the ideal value of 60 mV/decade at room temperature. However, after repeated annealing at 250 °C and 300 °C, each for 1 minute in N_2

gas, SS dramatically improved to 100 mV/decade (solid lines in Fig. 2). This is comparable to the best SS value (~ 90 mV/decade) reported for InAs NW-FETs [6]. The annealing also resulted in decreased on-current and increased threshold voltage. These observations suggest the formation of a tunnel-barrier in the channel, which blocks the thermionic diffusion of electrons in the subthreshold regime and improves SS [7, 8]. In fact, the formation of InAlAs alloy, having a wider band gap than InAs, was confirmed at the interface between the InAs NW and the Al source/drain electrodes by energy-dispersive X-ray spectroscopy analysis. We conclude that this alloy region is responsible for the SS improvement after annealing.

The above SS value of 100 mV/decade is slightly better than the smallest SS ~ 110 mV/decade obtained for our similar FETs using homogeneous InAs NW channels after annealing. This suggests an advantage of the InAs/InP core-shell NWs as a FET channel.

3. Conclusions

We have fabricated an encapsulated GAA InAs/InP core-shell NW-FET using self-aligned source/drain electrode stacks. Post-annealing improved SS to 100 mV/decade at room temperature, making it comparable to that of the best InAs NW-FETs. Our results demonstrate an advantage of using InAs/InP core-shell NWs as an FET channel combined with the post-annealing technique.

Acknowledgement

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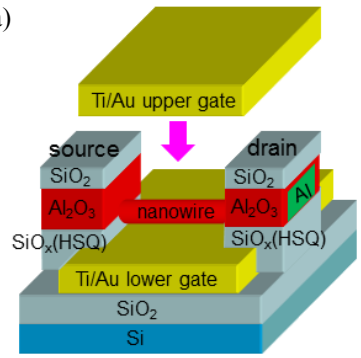
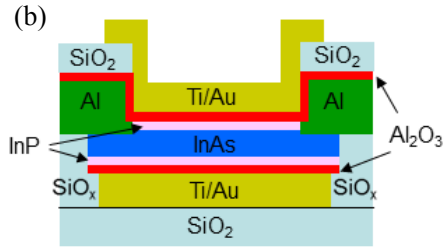
(a)



(b)



(c)

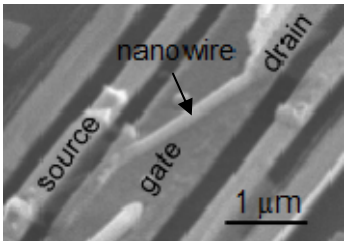


Fig. 1 (a) Schematic device structure of GAA NW-FET. (b) Schematic cross-section along the NW axis. (c) SEM image of the fabricated device.

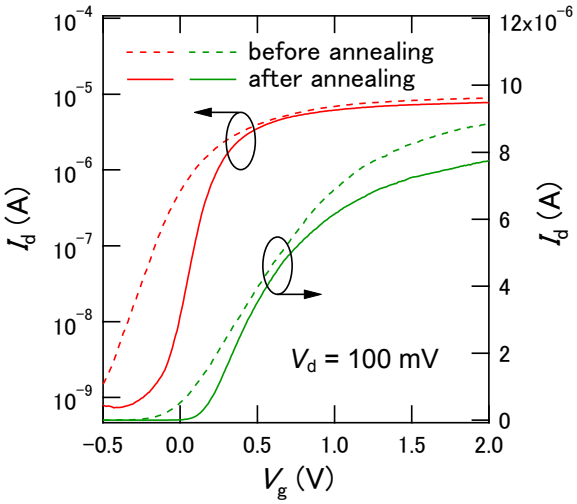


Fig. 2 $I_d - V_g$ characteristics for V_d = 100 mV before and after annealing.