Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp1038-1039

# Integration of Vertical InAs Nanowires on Ge(111) by Selective-Area MOVPE

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**Abstract**

**We report on selective-area growth of InAs nanowires (NWs) on Ge(111) substrates by using selective-area metal-organic vapor phase epitaxy (MOVPE) and discuss how to control the growth direction of InAs NWs on the Ge(111). Then, we characterize the electrical properties of the InAs nanowire/Ge heterojunctions for the electrical device application.**

## 1. Introduction

III-V compound semiconductor nanowires (NWs) have been attracted much attention for future electrical and optical device applications. Among them, InAs and InGaAs NWs are promising material as alternative channels for future n-type field-effect transistors (FETs) because these materials have fast electron mobility due to small electron effective mass, as well as good geometry for surrounding-gate architecture.

Silicon complementary metal-oxide-semiconductor (CMOS) technologies are exploring alternative channel materials such as III-Vs for n-channel [1] and Ge for p-channel MOSFETs [2], and new gate architecture such as gate-all-around (GAA) and surrounding-gate structures. In this regard, co-integration technique of the III-Vs and Ge on the same platform is very important for future Si-CMOS compatible process. For instance, wafer-bonding of InGaAs with Ge has been reported as one of co-integration techniques for III-V/Ge CMOS application so far [3].

Direct integration of vertical III-V NWs on Ge is promising co-integration technique. However, there have been few report regarding the selective-area growth of III-V NWs on Ge substrates [4], especially highly lattice mismatched system such as InAs NWs on Ge (lattice mismatch: 7.1 %) have not been reported. Here we report on a selective-area growth of InAs NWs on Ge(111) substrate and discuss solution of a polarity mismatch between the InAs and Ge to control the growth directions of InAs NWs into vertical directions on Ge(111).

## 2. Experiments

*2-1. Selective-Area MOVPE*

The n-type and p-type Ge(111) substrates were used for growth. 20 nm-thick $SiO_2$ or 15 nm-thick SiON were formed by using RF sputtering technique. Then, openings were formed using electron-beam (EB) lithography and dry/wet etchings. The openings were 90 nm in diameter for characterization of growth directions and 70 nm in diameter for current-voltage (I-V) characterizations. InAs NWs were grown by MOVPE with $H_2$ carrier gas. Trimethylindium (TMIn), and arsine ($AsH_3$) were used for growth materials. Monosilane ($SiH_4$) was used for n-type dopant and dimethylzinc (DEZn) was used for p-type dopant. The growth temperature was 560°C.

*2-2. Device process*

A two terminal device was fabricated for characterization of electrical properties in InAs NW/Ge interface by first coating the NWs with benzocycrobutene (BCB, DOW CHEMICAL) by spin-coating. Then, 500 nm length of InAs were revealed by reactive-ion etching (RIE) of the BCB layer using $O_2/CF_4$ mixed gas. Next, 20 nm-thick Ni/50 nm-thick Au was evaporated on top of the NWs and 15 nm-thick Ni was deposited on backside of the Ge substrates. The devices were annealed at 350°C for 3 min in $N_2$.

## *3. Results and discussion*

*3-1. Growth of vertical InAs NWs on Ge substrates*

Initial surface of non-polar Ge(111) should be modified into (111)B-polar surface to align vertical InAs NWs because the preferential growth direction of the InAs NWs is <111>B direction. First, we investigated the control of the polarity for Ge(111) surface during InAs NWs growth. The polarity of Ge(111) [(111)A or (111)B] was indentified from growth direction of grown InAs NWs. The growth of vertical InAs NW means initial Ge surface transferred into (111)B-polar surface, in which the outermost Ge atoms are replaced by As atoms (As-incorporated $Ge^{3+}$) or dangling-bond on outermost Ge atoms are terminated by In atoms (In-terminated $Ge^{1+}$). While those of tilted NWs stands for the formation of (111)A-polar Ge surface, in which the outermost Ge atoms are terminated by group V atoms (As-terminated $Ge^{1+}$).

Figure 1(a) shows the growth sequence for the growth of InAs NWs on Ge(111). After the Ge(111) was etched by buffered HF, the substrate was annealed at 600ºC in $H_2$ for 5 min. Then the substrate was cooled down to 400ºC and $AsH_3$ was supplied to form As-incorporated Ge(111) 1×1 surface for 5 min. Next, flow-rate modulation epitaxy (FME) was performed to terminate In atoms on the As-incorporated Ge(111) surface and dangling bonds on non-incorporated Ge atoms by As atoms. Then, InAs NW growth was resumed. Fig. 1(b) depicts the percentage of vertical InAs NWs with a variation of partial pressure of

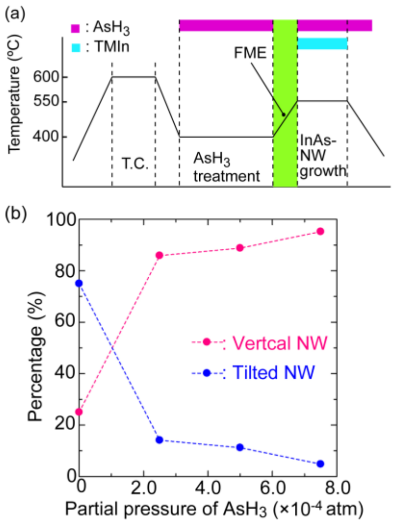


Fig. 1 (a) Growth sequence of InAs NWs on Ge(111). T. C. stands for thermal cleaning. (b) Percentage of vertical InAs NWs with a variation of [$AsH_3$].

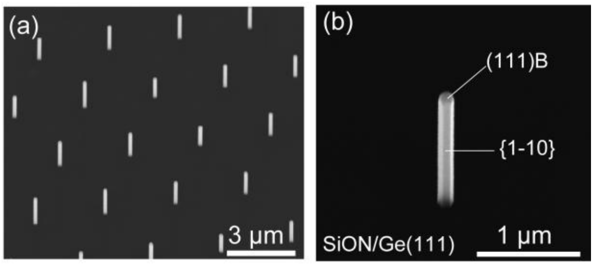


Fig. 2 (a) 30º-tilted SEM image of the vertical InAs NWs on SiON-masked Ge(111) substrate.(b) Magnified SEM image of the vertical InAs NW. The vertical side facets are {1-10}.

[$AsH_3$] during the $AsH_3$ surface treatment at 400ºC in Fig. 1(a). The yield of vertical NW was 25% when the [$AsH_3$] was zero, and increased with increasing [$AsH_3$]. This indicates the Ge(111) surface could be modified to (111)B-polar surface by the $AsH_3$ surface treatment at 400ºC. However, (111)A-polar surface (As-terminated $Ge^{1+}$) was simultaneously formed during the $AsH_3$ treatment because the 12% of tilted InAs NWs were remained at [$AsH_3$] = 5.0 × $10^{-4}$ atm. Thus, we changed the $AsH_3$ treatment time 10 min at [$AsH_3$] = 3.75 × $10^{-4}$ atm, which corresponds to 7.5 × $10^{-4}$ atm for 5 min. The percentage of the vertical InAs NWs was thus improved to 95% in Fig.1 (b).

The 5% of tilted InAs NWs were remained which caused from the contamination such as residual $SiO_x$ and process-induced fluctuation. Thus we changed the mask film from $SiO_2$ to SiON to suppress contaminations. Fig. 2(a) shows the representative SEM image of the vertical InAs NW array on SiON-masked Ge(111) substrate. The yield of the vertical InAs NWs was completely 100% and uniform hexagonal-shaped uniform InAs NWs were grown on the Ge(111) substrate. The average diameter was 70 nm which is same as that of openings, which means lateral growth was suppressed.

Current density-voltage (J-V) characteristic showed

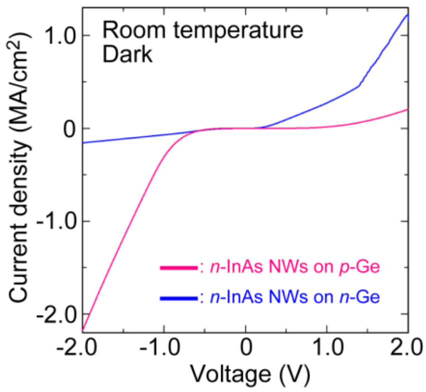


Fig. 3 Current density-voltage properties for *n*-InAs NWs on *p*-Ge and *n*-InAs NWs on *n*-Ge.

specific electrical properties. Fig. 3(a) depicts the J-V curve of Si-doped InAs NWs on *p*-Ge. In this case, the number of the InAs NWs was 250 and each NWs were 120 nm in diameter. The curve showed typical rectification under forward bias direction (-2.0 < V < 0) with an ideality factor of 1.3. Under the reverse bias direction, Zener tunneling current was observed. From this property, built-in voltage across the *n*-InAs NW and *p*-Ge was 0.31 V. Zn-doped InAs NWs on *n*-Ge substrate similarly shows rectification with a built-in potential of 0.3 V (not shows here). In contrast with these InAs/Ge heterojunctions, the J-V curve for *n*-InAs NWs/*n*-Ge indicated unique property. Fig. 3(b) depicts the J-V property for the *n*-InAs NWs/*n*-Ge heterojunction. The curve shows rectification properties although the electrode poses Ohmic contact. Under positive voltage, the sample shows rectification with sudden break down behavior at around 1.5 V. This indicated the *n*-InAs/*n*-Ge heterojunction had unique band discontinuity which is similar to typical p-n junction. Furthermore, the InAs/Ge heterojunction depicted a large avalanche break down under the lower positive bias. This unique behavior indicated a possibility for the use of voltage controlled switch with impact ionization FET and conventioanl FETs on same plarform.

## 4. Conclusions

We reported on a selective-area growth of InAs NWs on Ge(111) and how to control the growth directions of InAs NWs on Ge(111) for the first time. And electronic characteristic for the InAs NW/Ge heterojunctions showed specific band discontinuity.


## Acknowledgements

This work was financially supported by a Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology (MEXT) and the Japan Science and Technology Agency (JST) PRESTO program.


## References


[1] J. A. del Alamo, Nature **479** (2011) 317.
[2] R. Pillarisetty, Nature **479** (2011) 324.
[3] M. Yokoyama *et al.*, APEX **5** (2012) 076501.
[4] E. P. A. M. Bakkers *et al.*, Nature Mat. **3** (2004) 769.