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Impact of High-κ Spacers on Parasitic Effects Considering DC/AC Performance Optimization in Si-Nanowire FETs for sub 10 nm Technology Node

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Abstract

In this paper, we proposed the optimized high-κ spacer design information of Si-nanowire FETs for sub 10 nm technology node. Using well-calibrated TCAD simulations and analytic RC models, the impacts of dielectric constant (ϵ_{sp}) and extension length (L_{EXT}) of spacer were extensively investigated in DC/AC performance within various power supply voltage V_{dd}. Due to a trade-off between source/drain series resistances (R_{SD}) and parasitic capacitances (C_{para}), the optimum value of ϵ_{sp} for AC performances shifts to low-κ as L_{EXT} and V_{dd} decrease.

1. Introduction

In the silicon technology, the fin-based multi-gate field effect transistors (FinFETs) have been successfully applied to mass production in 22 nm technology node [1]. In many attempts for further scaling, high-κ spacer techniques have been considered and their effects on device performance have been reported in different structures such as junctionless transistors [2] and FinFETs [3]. However there are no enough researches about impacts of high-κ spacers applied to gate-all-around nanowire FETs (GAA NWFETs), which are the one of attractive candidates for sub 10 nm technology node. In this paper, effects of the dielectric constant (ϵ_{sp}) and device geometry on DC/AC performances are quantitatively evaluated various figure-of-merit (FOM) such as I_{on}/I_{off}, intrinsic delay (CV/I) and current-gain cutoff frequency (f_T). Finally the optimized geometry demonstrating the best performance of NWFETs are suggested.

2. Device Structure and Parasitic RC Extraction

The structure of Si-NWFET is built based on International Technology Roadmap for Semiconductors (ITRS) criterion [4], as shown in **Fig. 1**. Especially we carefully thought about pitch and parasitic capacitance of Gate-to-S/D, which are extremely critical to current 3D MOSFET design. **Table I** indicates our TCAD electrical data are very close to ITRS estimation in reasonable range. The source/drain (S/D) series resistance (R_{SD}) of NWFETs is composed of five major components: the spreading resistance (R_{SP}), the extension resistance (R_{EXT}), the S/D nanowire interface resistance (R_{INT}), the deep S/D resistance (R_{DP}), and the contact resistance (R_{CON}). R_{SD} and each component are calculated by an analytical model [5] and compared with the extracted R_{SD} by the Y-function technique [6] simultaneously. The calculated R_{SD} show excellent agreement with the extracted R_{SD} for all high-κ materials (inset of **Fig. 3**). In addition, bias-independent overlap capacitance (C_{ov_indep}) and bias-dependent overlap capacitance (C_{ov_dep}) are extracted from gate capacitance (C_{gg}) [7] to calculate CV/I. At last, f_T are extracted using simulated H-parameters where the current-gain drops to unity ($|H_{21}|=1$).

3. Results and Discussion

Fig. 2 shows the I_D-V_G characteristics of GAA NWFETs. The on current is boosted about 57 % using HfO_2 spacer instead of SiO_2. Also all devices show strong short channel effects immunity, i.e 61 mV/dec subthreshold slope due to excellent gate controllability of GAA structures. This I_D increase is attributed to R_{EXT}, R_{SP}, and R_{INT} decrease as ϵ_{sp} increases (**Fig. 3**). Especially, given that R_{SD}-R_{EXT} have nearly same value for different spacer materials (inset of **Fig. 3**), R_{EXT} reduction significantly contributes to R_{SD} decrease. In **Fig.4**, a higher electric field is induced by fringe electric field through the high-κ materials between the channel and extension region. As a result in **Fig. 5**, the electron concentration accumulated at the extension region increases and the resistivity of R_{SP}, R_{EXT}, and R_{INT} namely ρ_{SP} ρ_{EXT}, and ρ_{INT} decrease (inset of **Fig. 5**). This is the reason why R_{SD} decrease with high-κ spacers. C_{gg} is normalized with the circumstance of the channel of NWFETs and increases as ϵ_{sp} increases due to C_{para}, as shown in **Fig 6**. In **Fig 7**, we compared constant value of intrinsic capacitance (C_{int}), C_{ov_indep} and C_{ov_dep} linearly increase because C_{ov_indep} and C_{ov_dep} are directly proportional to ϵ_{sp} [8]. Due to trade-off between R_{SD} and C_{para}, optimization process is imperative in design of NWFETs. **Figs. 8 (a)** and **(b)** show the trend of f_T and CV/I as functions of V_{dd}, ϵ_{sp}, and L_{EXT}, which are important variables in device designs. As V_{dd} and L_{EXT} decrease, optimum points of f_T and CV/I shifts to low-κ materials and we put optimum materials in **Table II**.

4. Conclusion

The effects of high-κ spacers on parasitic RC of GAA NWFETs are investigated with different materials and thickness. High-κ spacers can improve DC performance remarkably with increased on current by reducing R_{SD}. Meanwhile, AC performance severely degraded due to increase of C_{para}. The optimum points of delay and f_T are suggested in various V_{dd} and L_{EXT}. Considering a trade-off between R_{SD} and C_{para}, optimized geometry is inevitable in design of NWFETs for sub 10nm technology node.

References

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Table I. Geometry Used in This Work

	ITRS (HP)	Simulation
Gate Pitch (nm)	64	64
Gate length (nm)	18	18
V_{dd} (V)	0.85	0.85
EOT (nm)	0.77	0.77
Channel doping (cm^{-3})	10^{17}	10^{17}
R_{SD} ($\Omega \cdot \mu m$)	146	144 ~ 220
C_{gg} (fF/μm)	1.1	0.85 ~ 1.6
C_{para} (fF/μm)	0.6	0.37 ~ 1.33

Table II. Optimized Spacer Materials for FOM

	L_{EXT} (nm)	V_{dd} (V) 0.65	0.7	0.75	0.8	0.85
f_T	10	SiO_2	SiO_2	SiO_2	SiO_2	Si_3N_4
	12	SiO_2	SiO_2	Si_3N_4	Si_3N_4	Al_2O_3
	14	SiO_2	Si_3N_4	Si_3N_4	Al_2O_3	Al_2O_3
	16	Si_3N_4	Al_2O_3	Al_2O_3	Y_2O_3	Y_2O_3
CV/I	10	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2
	12	SiO_2	SiO_2	SiO_2	Si_3N_4	Si_3N_4
	14	SiO_2	SiO_2	Si_3N_4	Si_3N_4	Si_3N_4
	16	SiO_2	Si_3N_4	Si_3N_4	Si_3N_4	Si_3N_4

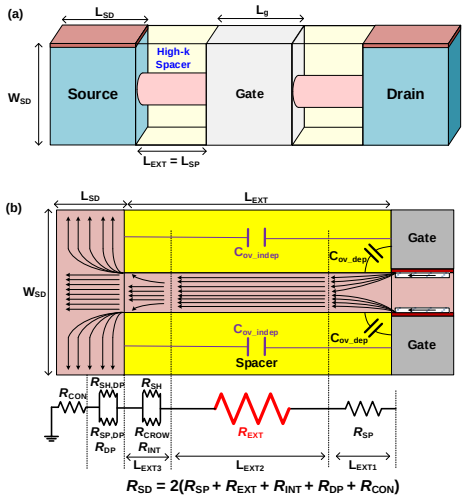

Fig. 1. (a) Three-dimensional schematic representation of NWFETs with high-κ spacers (b) Cross-sectional view of NWFETs with parasitic components descriptions [5],[8].

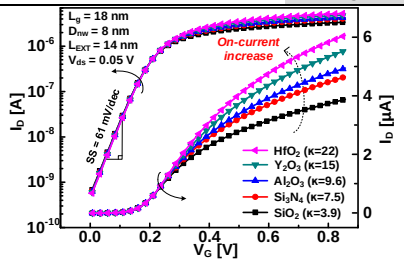

Fig. 2. The simulated I_D-V_G characteristics of NWFETs with different spacer dielectric materials.

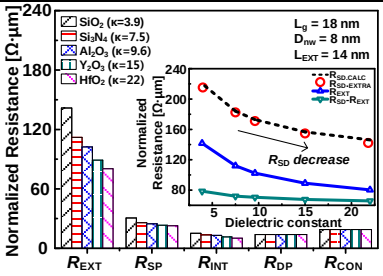

Fig. 3. R_{SD} components of NWFETs with high-κ spacers.

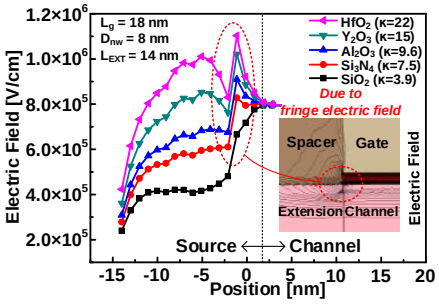

Fig. 4. Electric field comparison with different spacer materials.

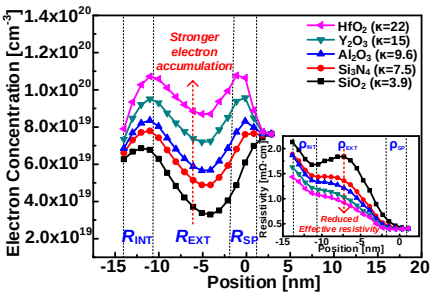

Fig. 5. Electron concentration and resistivity comparison with different spacer materials.

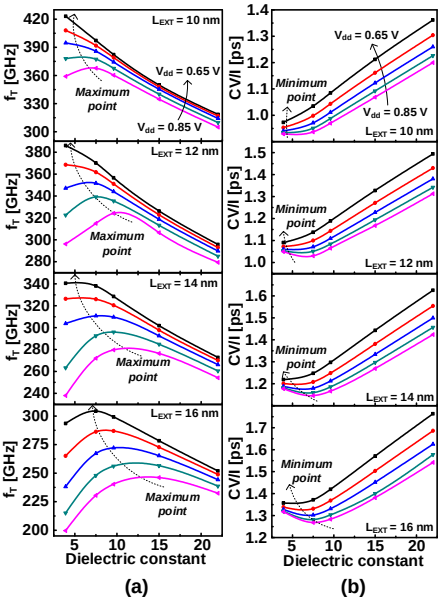

Fig. 8. (a) f_T (b) CV/I for different operation condition and L_{EXT}. As V_{dd} and L_{EXT} decrease, low-κ spacers show outstanding performances.

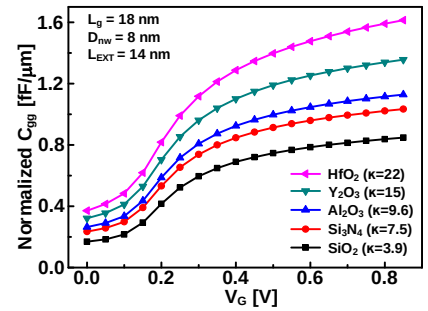

Fig. 6. Normalized C_{gg} with different spacer materials.

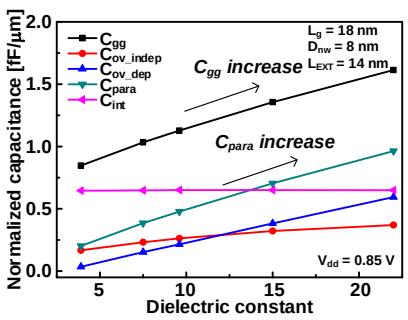

Fig. 7. Extracted parasitic overlap capacitances as a function of dielectric constant.