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Carbon Nanotube FETs for Robust Digital Logic Systems

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Abstract

Carbon nanotube (CNT)-based FETs are a promising nanotechnology for high performance and highly energy-efficient digital logic applications. It is projected that digital systems made from carbon nanotube FETs (CNFETs) can achieve a 10-fold improvement in energy-delay product, a metric of energy efficiency, versus silicon-CMOS [1,2]. However, substantial imperfections inherent to CNTs have prohibited CNFET circuit demonstrations. In this paper, we summarize advances that have enabled robust CNFET circuit demonstrations. We also highlight experimental demonstrations of CNFET digital systems, including the first CNT computer and monolithically integrated 3D circuits.

1. Imperfection-Immune Paradigm

CNTs are inherently subject to substantial imperfections that pose major obstacles to the design of robust and very large-scale CNFET digital systems. Two of these inherent imperfections are [3]:

1) Mis-positioned CNTs, which introduce stray conducting paths that can lead to incorrect logic functionality.

2) Metallic CNTs, which due to their diameter and chirality have little or no band-gap resulting in leakage current and incorrect logic functionality.

The overcome these obstacles, we rely on a unique combination of design and processing techniques known as the imperfection-immune paradigm [3]. For mis-positioned CNTs, we employ mis-positioned CNT-immune design [4]. An example of mis-positioned CNT-immune design for a NAND2 gate is shown in Figure 1, highlighting the etched regions within the design. These etched regions guarantee correct logic functionality despite the presence of any mis-positoned CNTs, while incurring minimal area, power, and speed cost at the chip-level [4]. Importantly, the etched regions are defined within the standard cells so there is no die-specific customization. It is therefore compatible with VLSI processing and design flows.

To overcome metallic CNTs, we use VLSI-compatible Metallic CNT Removal (VMR) [5]. VMR (process steps illustrated in Figure 2) is a design technique that allows electrical breakdown to be performed at the chip scale, and is also compatible with VLSI design and processing flows. VMR has been shown to remove >99.99% of all metallic CNTs, while only inadvertently removing <4% of semiconducting CNTs [5,8]. It has been shown that both mis-positioned CNT-immune design and VMR for selective removal of metallic CNTs can be applied to highly-scaled CNFETs with sub-20 nm channel lengths [6].

2. Digital Systems Demonstrations

The imperfection-immune paradigm has enabled experimental demonstrations of robust CNFET digital circuits [7,8], including the first basic processor built entirely using CNFETs (Figure 3). This processor has 178 CNFETs with >30,000 CNTs, demonstrating the ability to manufacture larger-scale CNFET circuits [9]. As a demonstration, the processor performed multi-tasking, by executing integer counting and integer sorting concurrently, in an interleaved fashion (Figure 4). To further demonstrate its flexibility, the processor emulated 20 different instructions from the commercial MIPS instruction set. Most importantly, the CNT computer demonstrated the ability to form any arbitrary digital system using CNFETs, with a maximum of 7 stages of cascaded combinational and sequential logic.

3. Monolithic 3D Integrated Circuits

An exciting application of CNFET digital systems is monolithic 3D ICs. Monolithic 3D ICs are an attractive technology option because they enable a very high density of Inter-Layer Vias (ILVs) compared to Through-Silicon Vias (TSVs) (Figure 5) [10]. CNFETs enable monolithic 3D ICs due to their low-processing temperature, and multiple layers of cascading complementary logic has been experimentally demonstrated [11]. Additionally, monolithic 3D integration of CNFETs on a silicon-CMOS substrate has been demonstrated (Figure 6) [12].

4. Conclusion

CNFETs are an exciting emerging nanotechnology that promise both increased performance and energy efficiency. By employing the imperfection-immune paradigm, larger-scale and increasingly complex circuit demonstrations are possible, as demonstrated by the first CNT computer. Monolithic 3D ICs represent another promising application that is enabled by CNFETs. While progress ranging from improving CNT contact resistance to robust CNT doping techniques to increasing CNT density must be made, promising work to overcome all of these obstacles has been demonstrated [12-14]. Thus CNFETs are positioned as an exciting and feasible next-generation technology to supplement silicon-CMOS.

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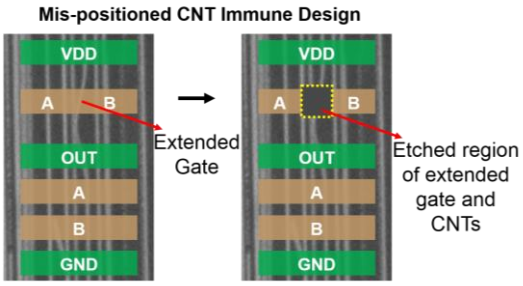

Figure 1. Mis-positioned CNT-immune design for a NAND2. An etch region defined within the standard cell renders the logic gate immune to any mis-positioned CNTs.

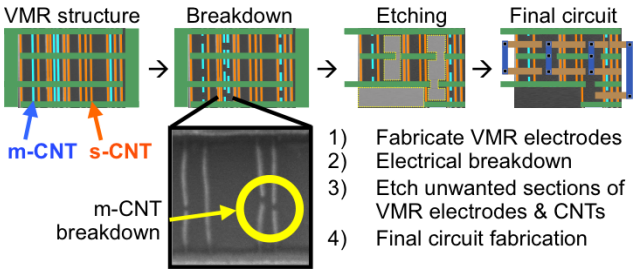

Figure 2. Schematic illustrations of VMR design and process flow. Details of the process can be found in [5].

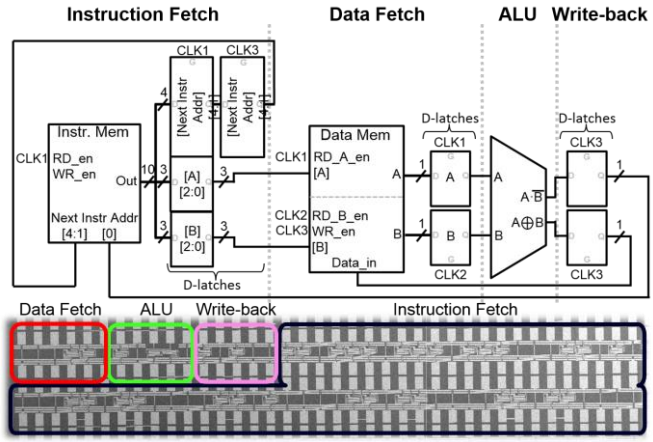

Figure 3. CNT computer. Top: schematic of CNT computer, composed of 4 sub-units: instruction fetch, data fetch, arithmetic unit (ALU), and write-back stage. Bottom: Scanning electron microscopy image of a CNT computer.

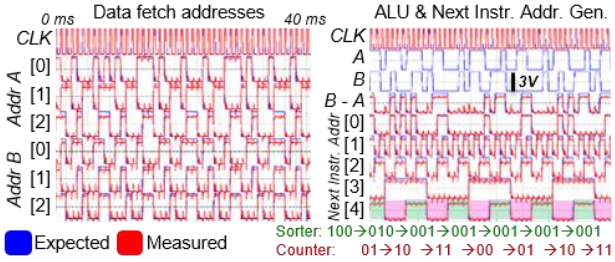

Figure 4. CNT computer output waveform, showing correct operation. This waveform shows the computer performing integer sorting and integer counting concurrently. The CNT computer implements non-pre-emptive multi-tasking, whereby each process voluntarily performs a self-interrupt and gives control to the other task.

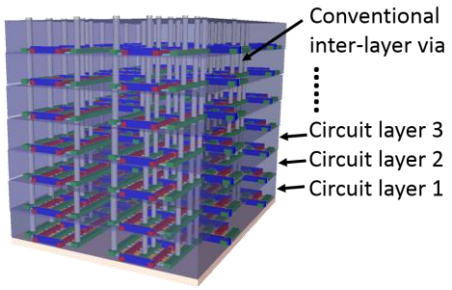

Figure 5. Schematic of a monolithic 3D IC. Multiple layers of circuits are fabricated directly over previous layer of circuits, using the same substrate. The circuit layers are connected with minimum-size vias rather than larger TSVs.

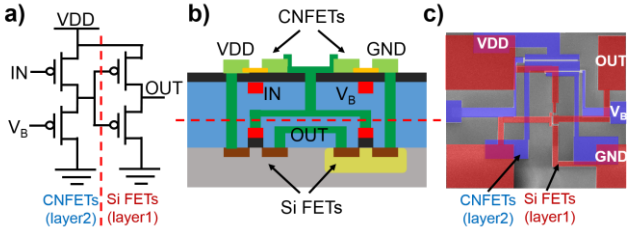

Figure 6. Monolithic 3D integration of CNFETs on a silicon-CMOS substrate. (a) schematic of cascaded inverters, with the 1st inverter implemented with CNFETs on the 2nd layer of circuits, and the 2nd inverter implemented with silicon-CMOS on the 1st layer of circuits. (b) cross-sectional view of CNFETs fabricated directly over silicon-CMOS, connected using inter-layer vias. (c) Scanning electron microscopy image of the fabricated circuit shown in (a-b).

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