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# Wafer Scale Fabrication of Transistors using CVD-Grown Graphene and its Application to Inverter Circuit

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**Abstract**

**Graphene transistors were fabricated with a wafer scale "top-down" process using a graphene sheet formed by the chemical vapor deposition (CVD) method. The devices have a dual-gated structure with an ion-irradiated channel, in which transistor polarity can be electrostatically controlled. We demonstrated inverter operation in a six-terminal device which was constructed by the combination of two dual-gated devices.**

## 1. Introduction

Graphene has been expected as a future electronics material, and much effort has been devoted to the application of graphene to a channel material in advanced LSIs. The lack of band gap, however, has been the most serious bottleneck [1]. In order to overcome this bottleneck, we proposed our original concept of dual-gated graphene transistors before [2] (Fig. 1). This type of device, as well as the other types of transistors using graphene nanoribbons or bilayer graphene, was demonstrated only on micrometer-sized graphene flakes obtained by mechanical exfoliation, which is not feasible for the industrial mass fabrication. In this work, we present the wafer scale fabrication of transistors (Fig. 2(a)) using graphene grown by the chemical vapor deposition (CVD) method [3], and demonstrate the transistor operations.

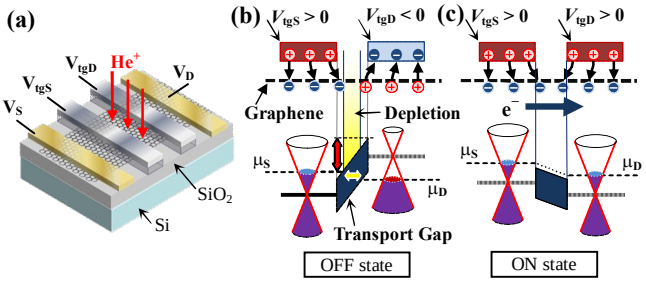


Fig. 1 (a) Schematic illustration of dual-gated graphene transistor with a helium ion irradiated graphene channel. It has source and drain contacts and a pair of top gates. The region between these two top gates was irradiated with an helium ion beam in order to generate a transport gap. (b) Off state of the transistor is realized by applying gate biases of opposite polarities to each other. In this configuration, depleted region will appear in the central part of the channel, which works as a high and long barrier to the carriers. (c) ON state is obtained by applying the gate biases of the same polarity.

## 2. Device Fabrication

A graphene sheet grown by the CVD method on a Cu-film surface at 1000 was transferred to a 3 inch Si wafer with a 285-nm-thick $SiO_2$ surface layer. After annealing for surface cleaning, each graphene device was isolated by photolithography and oxygen plasma etching as indicated by broken lines in Fig. 2(b). Source/drain contacts were processed by photolithography and lift-off methods with the thickness of Ti/Au = 5/25 nm. Top gates were fabricated by the e-beam lithography method, making a split-gate structure with a gap width of 20 nm. The gate stack consisted of $SiO_2$/Al = 10/25 nm, which is seen as white regions in Fig. 2(b). The $SiO_2$ layer was inserted in order to increase the distance between the Al electrodes and the graphene layer so that the top gate can control the electrostatic potential of graphene between the gates. The region between the top gates was irradiated with a helium ion beam using a helium ion microscope [4,5]. In this work, this irradiated region is referred to as ñchannelò. The ion

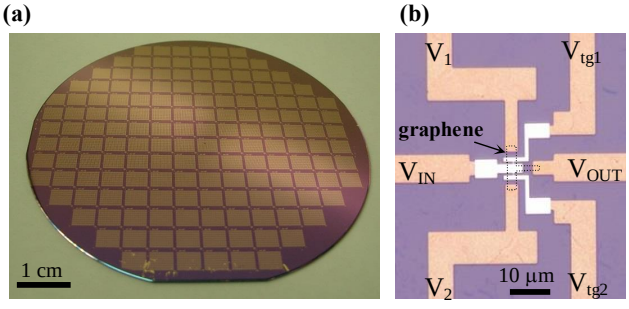


Fig. 2 (a) A picture of fabricated devices on a 3 inch wafer. (b) An image of a triple-gated device. Broken lines indicate the position of graphene.

dose in the channel was $8\times10^{-15}$ ions/cm$^2$, which corresponds to the defect density of 0.8% [4]. The length, $L$, and the width, $W$, of the channel were designed to be $W/L$ = 50/20 nm. It should be noted that one of the important features of this device concept is that this device fabrication process is totally a ñtop-downò one. In the present work, we used a helium ion microscope for the channel irradiation, but it can easily be replaced by the combination of photo lithography and ion implantation.

## 3. Device Operation

The operation principle of our dual-gated transistor is explained in Fig. 1(b) and (c), and it was already reported elsewhere [2]. In this device concept, the transistor polarity (n- or p-type) is determined by the bias polarity of one of the gates. In this study, we applied this concept to an inverter circuit shown in Fig. 2(b). Figure 3 explains the circuit structure. Two dual-gated devices are connected to form an inverter where $V_1$ and $V_2$ are at high and low levels, respectively, while the gate-bias polarities are $V_{tg1} < 0$ and $V_{tg2} > 0$ (Fig. 3(a)). In these devices, two of inner gates can be combined, forming a triple-gated device shown in Fig. 3(b), which is equivalent to the inverter shown in Fig. 3(a). Figure 3(c) is the circuit diagram of the inverter with two

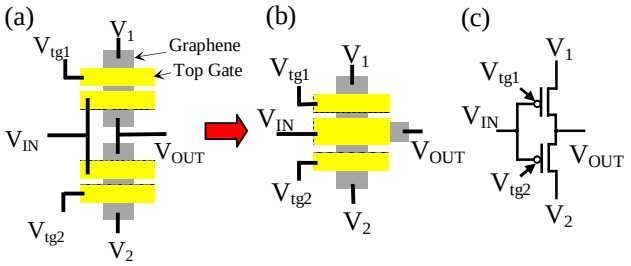


Fig. 3 Device structure with triple gates. (a) Two dual-gated transistors are combined to form an inverter circuit. The inner two gates can be merged to one. (b) Triple-gated device with three contacts. This six-terminal device works as an inverter as shown in (c). Here, the polarity of each transistor is controlled by the gate biases of $V_{tg1}$ or $V_{tg2}$.

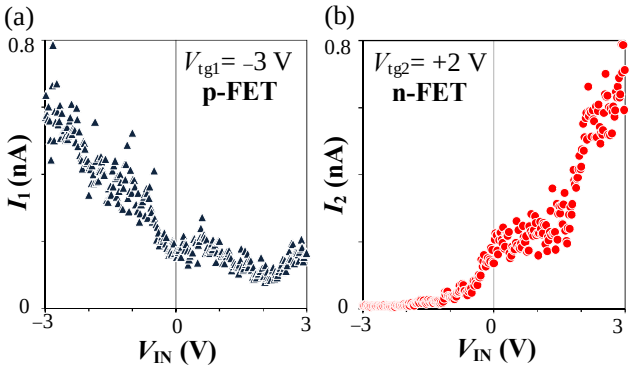


Fig. 4 Transistor operation in the device shown in Fig. 3(b) at $V_1 = V_2 = +100$ mV, $V_{OUT} = -100$ mV and at $T = 200$ K. Current $I_1$ flows from $V_1$ to $V_{OUT}$, and $I_2$ flows from $V_2$ to $V_{OUT}$. (a) $V_{tg1} < 0$ makes the upper part a p-type FET for the sweeping of $V_{IN}$. (b) In the lower part, $V_{tg2} > 0$ makes it an n-type FET.

polarity reversible transistors.

Independent operation of the two transistors in Fig. 3 was performed simultaneously at the biases of $V_1 = V_2 = +100$ mV, $V_{OUT} = -100$ mV, $V_{tg1} = -3$ V and $V_{tg2} = +2$ V at $T = 200$ K. Here, $I_1$ and $I_2$ are the currents from $V_1$ to $V_{OUT}$ and $V_2$ to $V_{OUT}$, respectively, which were modulated by $V_{IN}$ as shown in Fig. 4. In this case, the upper and lower transistors in Fig. 3(b) worked as p- and n-type FETs, respectively, as the gate bias of $V_{IN}$ was swept.

Inverter operation was demonstrated in this device with the biases of $V_1 = +100$ mV, $V_2 = -100$ mV, $V_{tg1} = -3$ V and $V_{tg2} = +2$ V (Fig. 5(a)). Here, $V_{OUT}$ was measured with a high impedance voltage meter, and $V_{IN}$ was swept from –3 V to 3 V. As shown in Fig. 5(b), when $V_{IN} < 0$, the output voltage was close to $V_1$ because the upper transistor (p-FET) was the ON state and the lower transistor (n-FET) was the OFF state. On the other hand, in the case of $V_{IN} > 0$, the lower device (n-FET) became the ON state, and $V_{OUT}$ has the voltage close to $V_2$. Thus, the device works as an inverter. For the better performance with a better gain and higher operating temperature, more effort in energy gap engineering is still required.

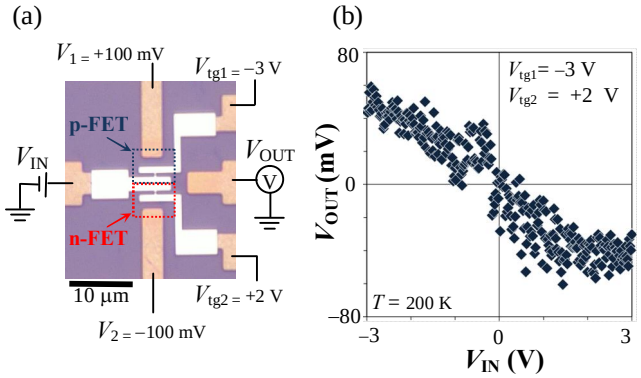


Fig. 5 (a) Bias configuration of the fabricated graphene inverter. In this case, the upper dual-gated transistor is a p-FET, and the lower one is an n-FET. (b) An inverter operation of the six-terminal device at $T = 200$ K.

## 4. Summary

Wafer scale fabrication of graphene transistors using CVD grown graphene was performed with a top-down process, and inverter operation in a fabricated six-terminal graphene device was demonstrated.


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